FPGA FOUNDATIONS

Complete Curriculum Review

27 chapters - 283 lessons - 10 guided activities and 10 randomized checks per lesson

A written evaluation catalog covering the learning objective, example, learner action, teaching aid, lab evidence, signal model, and physical Microchip FPGA board path for every lesson.

Testing curriculum - all levels currently enabled

How to evaluate this document

This catalog mirrors the current in-app curriculum. Reviewers can evaluate continuity, prerequisite order, terminology, teaching depth, laboratory authenticity, assessment quality, and hardware feasibility without opening each lesson individually.

Implementation status: lesson text and guided activity tracks are available in the app. Advanced signal diagrams are conceptual teaching aids, not execution of the learner's HDL. Activities that require an HDL simulator, Libero, or a physical board must be completed with those external tools. Source exports are starter packages with unresolved board pins, not ready-to-flash images. Hardware paths describe intended verification; this catalog does not certify that every lab has been synthesized or run on a board. The 50-item question banks use generated variants of the lesson material, not 50 independently authored problems.

Review dimension	Question for the reviewer
Sequence	Does each lesson rely only on concepts introduced earlier?
Clarity	Can a new learner state the required action without guessing?
Practice	Do ten labs move from guided observation to independent construction?
Assessment	Do ten randomized checks test understanding rather than memorization?
Evidence	Is the expected waveform, report, or board observation explicit?
Hardware	Can the activity be reproduced on the named Microchip FPGA board?
Safety	Are clock, I/O, programming, security, and electrical assumptions controlled?

Curriculum architecture

Chapter	Lessons	Outcome
0 - Digital Logic Pre-course	23	Optional preparation: learn 0/1 signals, truth tables, AND, OR, and NOT before FPGA design.
1 - Meet the FPGA	10	Understand what is being built before writing code.
2 - Read Verilog	10	Recognize the parts of a small hardware description.
3 - Write and Simulate	10	Create a complete small design and prove its behavior.
4 - Build Clocked RTL	10	Understand registers, clocks, reset, and state.
5 - Map RTL into an FPGA	10	Connect HDL concepts to physical FPGA resources.
6 - Put It on the PolarFire Board	10	Complete the real Libero-to-board workflow.
7 - Combinational Verilog	10	Write reusable combinational RTL without accidental storage.
8 - Sequential RTL	10	Design deterministic state, counters, enables, and finite-state machines.
9 - Verification Engineering	10	Build self-checking simulations that detect errors automatically.
10 - Pipelines, Handshakes, and CDC	10	Move data safely through high-performance and multi-clock systems.
11 - Memories and DSP	10	Use FPGA memory blocks and arithmetic resources effectively.
12 - Timing and Constraints	10	Constrain clocks and interfaces, then interpret timing reports correctly.
13 - Digital Interfaces	10	Implement and verify common board and peripheral protocols.
14 - PolarFire Architecture	10	Map RTL decisions onto Microchip PolarFire resources.
15 - Libero SoC Workflow	10	Take a reviewed RTL design through Microchip implementation tools.
16 - Capstone FPGA Systems	10	Combine design, verification, timing, and board evidence in complete projects.
17 - Advanced SystemVerilog RTL	10	Build strongly typed, reusable, reviewable hardware modules.
18 - Clocking, Reset, and CDC	10	Engineer clocks, resets, and safe transfers between timing domains.
19 - Verification and Formal Reasoning	10	Create self-checking, coverage-driven, assertion-based verification.
20 - High-Speed I/O and Transceivers	10	Bring up serial links and measure their integrity on supported hardware.
21 - External Memory and Data Movement	10	Control memory, buffering, arbitration, and high-throughput transfers.
22 - PolarFire SoC and RISC-V Integration	10	Connect FPGA fabric with the PolarFire SoC microprocessor subsystem.
23 - Power, Thermal, and Reliability Engineering	10	Measure and improve power efficiency, robustness, and recoverability.
24 - FPGA Security and Provisioning	10	Protect configuration, debug access, keys, and the device lifecycle.
25 - Professional FPGA Capstone	10	Deliver a traceable design from requirements through measured hardware.
26 - Real Board Project Studio	10	Build, simulate, constrain, and document ten original FPGA designs for the Microchip PolarFire SoC Discovery Kit.

0 - Digital Logic Pre-course

Optional preparation: learn 0/1 signals, truth tables, AND, OR, and NOT before FPGA design.

Lesson 001 - 0.1 - Signals: 0 and 1

Theme and objective	A digital signal has a name and a value. Here, 0 means LOW and 1 means HIGH. Each exercise gives the input and asks for one exact output.
Complete example	`A = 0 -> Y = 0` `A = 1 -> Y = 1`
Learner action	The circuit directly connects A to Y. If A is 1, what exact value must Y have?
Expected knowledge	Y = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Signals: 0 and 1
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, Y	Interactive inputs: A
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 002 - 0.2 - AND: both inputs required

Theme and objective	AND produces Y=1 only when both A and B are 1. Every other input pair produces Y=0.

Complete example	`A B | Y`
	`0 0 | 0`
	`0 1 | 0`
	`1 0 | 0`
	`1 1 | 1`

Learner action	Use the complete truth table. For A=1 and B=0, select the required output.
Expected knowledge	Y = 0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe AND: both inputs required
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 003 - 0.3 - OR: either input is enough

Theme and objective	OR produces Y=1 when either input is 1. It produces Y=0 only when both inputs are 0.

Complete example	`A B | Y`
	`0 0 | 0`
	`0 1 | 1`
	`1 0 | 1`
	`1 1 | 1`

Learner action	Use the complete truth table. For A=0 and B=1, select the required output.
Expected knowledge	Y = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe OR: either input is enough
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 004 - 0.4 - NOT: invert one input

Theme and objective	NOT reverses one input: when A is 0, Y is 1; when A is 1, Y is 0.

Complete example	`A | Y`
	`0 | 1`
	`1 | 0`

Learner action	Use the table. For A=1, what exact output is produced?
Expected knowledge	Y = 0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe NOT: invert one input
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, Y	Interactive inputs: A
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 005 - 0.5 - NAND: inverted AND

Theme and objective	NAND means NOT-AND: Y is 0 only when both A and B are 1. Its ANSI symbol is an AND gate with an inversion bubble at the output.

Complete example	`Y = NOT(A AND B)`
	`A B | Y`
	`0 0 | 1`
	`0 1 | 1`
	`1 0 | 1`
	`1 1 | 0`

Learner action	For A=1 and B=1, what output does NAND produce?
Expected knowledge	Y = 0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe NAND: inverted AND
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 006 - 0.6 - NOR: inverted OR

Theme and objective	NOR means NOT-OR: Y is 1 only when both A and B are 0. Its ANSI symbol is an OR gate with an inversion bubble at the output.

Complete example	`Y = NOT(A OR B)`
	`A B | Y`
	`0 0 | 1`
	`0 1 | 0`
	`1 0 | 0`
	`1 1 | 0`

Learner action	For A=0 and B=0, what output does NOR produce?
Expected knowledge	Y = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe NOR: inverted OR
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 007 - 0.7 - XOR: inputs are different

Theme and objective	XOR produces Y=1 when A and B are different. Its ANSI symbol is an OR shape with one additional curved line on the input side.

Complete example	`Y = A XOR B`
	`A B | Y`
	`0 0 | 0`
	`0 1 | 1`
	`1 0 | 1`
	`1 1 | 0`

Learner action	For A=1 and B=0, what output does XOR produce?
Expected knowledge	Y = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe XOR: inputs are different
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 008 - 0.8 - XNOR: inputs are equal

Theme and objective	XNOR is inverted XOR: Y=1 when A and B are equal. Its ANSI symbol adds an output inversion bubble to the XOR symbol.

Complete example	`Y = NOT(A XOR B)`
	`A B | Y`
	`0 0 | 1`
	`0 1 | 0`
	`1 0 | 0`
	`1 1 | 1`

Learner action	For A=1 and B=1, what output does XNOR produce?
Expected knowledge	Y = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe XNOR: inputs are equal
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, Y	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 009 - 0.9 - Multiplexer: choose one input

Theme and objective	A 2:1 multiplexer sends A to Y when select S=0, and sends B to Y when S=1.

Complete example	`A B S | Y`
	`0 0 0 | 0`
	`0 1 0 | 0`
	`1 0 0 | 1`
	`1 1 0 | 1`
	`0 0 1 | 0`
	`0 1 1 | 1`
	`1 0 1 | 0`
	`1 1 1 | 1`

Learner action	With S=1 and B=0, what is Y?
Expected knowledge	Y = 0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Multiplexer: choose one input
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A, B, S, Y	Interactive inputs: A, B, S
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 010 - 0.10 - Demultiplexer: route one input

Theme and objective	A demultiplexer sends one input D to exactly one selected output; the other output is 0.

Complete example	`D S | Y0 Y1`
	`0 0 | 0 0`
	`1 0 | 1 0`
	`0 1 | 0 0`
	`1 1 | 0 1`

Learner action	With S=1 and D=1, what is Y1?
Expected knowledge	Y1 = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Demultiplexer: route one input
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: D, S, Y0, Y1	Interactive inputs: D, S
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 011 - 0.11 - Decoder: binary to one-hot

Theme and objective	A 2-to-4 decoder activates exactly one output for each two-bit input.

Complete example	`A1 A0 | Y3 Y2 Y1 Y0`
	`0 0 | 0 0 0 1`
	`0 1 | 0 0 1 0`
	`1 0 | 0 1 0 0`
	`1 1 | 1 0 0 0`

Learner action	Which output is active for input 10?
Expected knowledge	Y2
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Decoder: binary to one-hot
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A1, A0, Y0, Y1, Y2, Y3	Interactive inputs: A1, A0
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 012 - 0.12 - Encoder: one-hot to binary

Theme and objective	An encoder performs the reverse operation: the active input position becomes a binary code.

Complete example	`D3 D2 D1 D0 | Y1 Y0`
	`0 0 0 1 | 0 0`
	`0 0 1 0 | 0 1`
	`0 1 0 0 | 1 0`
	`1 0 0 0 | 1 1`

Learner action	If D3 is active, what code is produced?
Expected knowledge	11
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Encoder: one-hot to binary
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: D0, D1, D2, D3, Y1, Y0	Interactive inputs: D0, D1, D2, D3
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 013 - 0.13 - 8:1 multiplexer: eight data inputs

Theme and objective	An 8:1 multiplexer uses three select bits S2:S0 to connect exactly one of D0 through D7 to Y.

Complete example	`S2 S1 S0 | Y`
	`0 0 0 | D0`
	`0 0 1 | D1`
	`0 1 0 | D2`
	`0 1 1 | D3`
	`1 0 0 | D4`
	`1 0 1 | D5`
	`1 1 0 | D6`
	`1 1 1 | D7`

Learner action	When S2:S0 = 101, which input is connected to Y?
Expected knowledge	D5
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe 8:1 multiplexer: eight data inputs
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: D0, D1, D2, D3, D4, D5, D6, D7, S2, S1, S0, Y	Interactive inputs: D0, D1, D2, D3, D4, D5, D6, D7, S2, S1, S0
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 014 - 0.14 - 1:8 demultiplexer: eight outputs

Theme and objective	A 1:8 demultiplexer uses S2:S0 to route D to one of eight outputs. All unselected outputs remain 0.

Complete example	`S2:S0=000 -> Y0=D`
	`001 -> Y1=D`
	`010 -> Y2=D`
	`011 -> Y3=D`
	`100 -> Y4=D`
	`101 -> Y5=D`
	`110 -> Y6=D`
	`111 -> Y7=D`

Learner action	With D=1 and S2:S0=110, which output becomes 1?
Expected knowledge	Y6
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe 1:8 demultiplexer: eight outputs
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: D, S2, S1, S0, Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	Interactive inputs: D, S2, S1, S0
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 015 - 0.15 - 3-to-8 decoder: eight one-hot outputs

Theme and objective	A 3-to-8 decoder converts A2:A0 into eight one-hot outputs. Exactly one of Y0 through Y7 is active.
Complete example	`A2:A0=000->Y0 001->Y1 010->Y2 011->Y3` `100->Y4 101->Y5 110->Y6 111->Y7`
Learner action	Which output is active when A2:A0=111?
Expected knowledge	Y7
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe 3-to-8 decoder: eight one-hot outputs
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: A2, A1, A0, Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	Interactive inputs: A2, A1, A0
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 016 - 0.16 - 8-to-3 encoder: eight one-hot inputs

Theme and objective	An 8-to-3 encoder converts one active input D0 through D7 into a three-bit binary output Y2:Y0.
Complete example	`D0->000 D1->001 D2->010 D3->011` `D4->100 D5->101 D6->110 D7->111`
Learner action	If D6 is the active input, what code is produced?
Expected knowledge	110
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe 8-to-3 encoder: eight one-hot inputs
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: D0, D1, D2, D3, D4, D5, D6, D7, Y2, Y1, Y0	Interactive inputs: D0, D1, D2, D3, D4, D5, D6, D7
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 017 - 0.17 - ALU: select an operation

Theme and objective	An arithmetic logic unit computes a selected operation such as add, subtract, AND, or OR.

Complete example	`OP1 OP0 | FUNCTION`
	`0 0 | A AND B`
	`0 1 | A OR B`
	`1 0 | A + B`
	`1 1 | A XOR B`
	
	`For ADD: A=2, B=3 -> Y=5`

Learner action	For ADD with A=2 and B=3, select Y.
Expected knowledge	5
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe ALU: select an operation
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: OP1, OP0, A0, B0, Y0, CARRY	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 018 - 0.18 - 8-bit ALU: buses, result, and flags

Theme and objective	An 8-bit ALU accepts A[7:0], B[7:0], and operation controls. It produces Y[7:0] plus status such as carry and zero.
Complete example	`OP=ADD, A=11111111, B=00000001` `Y=00000000, CARRY=1, ZERO=1`
Learner action	What carry is produced by 255 + 1 in an 8-bit ALU?
Expected knowledge	CARRY = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe 8-bit ALU: buses, result, and flags
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 019 - 0.19 - D flip-flop: capture one bit

Theme and objective	A D flip-flop copies D to Q only at its active clock edge, then holds Q steady between edges.
Complete example	`At rising CLK: Q(next) = D` `Between edges: Q holds its value`
Learner action	D is 1 at the rising edge. What does Q become?
Expected knowledge	Q = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe D flip-flop: capture one bit
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: D
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 020 - 0.20 - T flip-flop: toggle state

Theme and objective	At an active clock edge, a T flip-flop holds when T=0 and toggles Q when T=1.

Complete example	`T | Q(next)`
	`0 | Q (hold)`
	`1 | NOT Q (toggle)`

Learner action	Q is 0 and T=1 at the clock edge. What is Q next?
Expected knowledge	Q = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe T flip-flop: toggle state
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, T, Q	Interactive inputs: T
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 021 - 0.21 - JK flip-flop: set, reset, and toggle

Theme and objective	A JK flip-flop holds for 00, resets for 01, sets for 10, and toggles for 11 at the active edge.

Complete example	`J K | Q(next)`
	`0 0 | hold`
	`0 1 | 0`
	`1 0 | 1`
	`1 1 | toggle`

Learner action	Q is 1 and J=K=1 at the edge. What is Q next?
Expected knowledge	Q = 0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe JK flip-flop: set, reset, and toggle
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, J, K, Q	Interactive inputs: J, K
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 022 - 0.22 - SR flip-flop: set and reset

Theme and objective	A clocked SR flip-flop holds for S=R=0, sets for S=1,R=0, and resets for S=0,R=1. S=R=1 is forbidden in the basic form.

Complete example	`S R | Q(next)`
	`0 0 | hold`
	`0 1 | 0`
	`1 0 | 1`
	`1 1 | forbidden`

Learner action	For S=1 and R=0 at the edge, what does Q become?
Expected knowledge	Q = 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe SR flip-flop: set and reset
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, S, R, Q	Interactive inputs: S, R
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 023 - 0.23 - Register: store a value

Theme and objective	A register stores a multi-bit value at a clock edge and keeps it until the next enabled edge.
Complete example	`Before edge: D=1010` `At edge: Q becomes 1010`
Learner action	What does Q hold immediately after the edge?
Expected knowledge	1010
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Register: store a value
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D7, D6, D5, D4, D3, D2, D1, D0, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

1 - Meet the FPGA

Understand what is being built before writing code.

Lesson 024 - 1.1 - What is an FPGA?

Theme and objective	An FPGA is a chip containing configurable logic and connections. You describe a circuit, and design tools configure the chip to become that circuit.
Complete example	`A switch can become an input. Logic inside the FPGA can process it. An LED can show the output.`
Learner action	Select the statement that describes an FPGA.
Expected knowledge	A chip configured to implement a digital circuit
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe What is an FPGA?
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 025 - 1.2 - Hardware is not software

Theme and objective	Software instructions usually execute in sequence. FPGA logic operates in parallel: several hardware blocks can react at the same time.
Complete example	`Two counters implemented in an FPGA can count simultaneously because each counter is its own hardware.`
Learner action	Which behavior demonstrates parallel hardware?
Expected knowledge	Two independent counters update on the same clock edge
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Hardware is not software
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 026 - 1.3 - The complete design flow

Theme and objective	A usable FPGA design moves through a visible chain: describe, simulate, synthesize, place and route, generate a programming image, program, and test.
Complete example	`Verilog -> simulation waveform -> synthesized circuit -> placed FPGA resources -> programming file -> board.`
Learner action	Choose the correct first action.
Expected knowledge	Describe the intended circuit
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe The complete design flow
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 027 - 1.4 - FPGA fabric and hard blocks

Theme and objective	FPGA fabric contains LUT logic, flip-flops, routing, memories, DSP blocks, clock networks, and I/O resources. Each resource solves a different hardware need.
Complete example	`A Boolean equation uses a LUT; a sampled result uses a flip-flop; a multiply can use a DSP block.`
Learner action	Which resource stores one sampled bit?
Expected knowledge	A flip-flop
Teaching aid	FPGA FABRIC AND HARD BLOCKS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify fpga fabric and hard blocks
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for FPGA fabric and hard blocks

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 028 - 1.5 - Configuration and nonvolatile behavior

Theme and objective	Configuration defines the circuit implemented by programmable resources. PolarFire devices retain nonvolatile configuration, but a design still requires a controlled programming flow.
Complete example	`The same programmed image reconstructs the verified fabric design after power is restored.`
Learner action	What determines the circuit implemented in the FPGA fabric?
Expected knowledge	The verified configuration image
Teaching aid	CONFIGURATION AND NONVOLATILE BEHAVIOR - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify configuration and nonvolatile behavior
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Configuration and nonvolatile behavior

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 029 - 1.6 - Parallel circuits and concurrency

Theme and objective	Independent FPGA circuits operate concurrently. A UART, counter, and PWM engine can all respond during the same clock cycle.
Complete example	`One clock edge updates three separate state machines without a software scheduler.`
Learner action	Why can three blocks update on the same edge?
Expected knowledge	Each block is implemented as dedicated hardware
Teaching aid	PARALLEL CIRCUITS AND CONCURRENCY - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify parallel circuits and concurrency
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Parallel circuits and concurrency

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 030 - 1.7 - Combinational versus sequential hardware

Theme and objective	Combinational outputs depend on current inputs. Sequential hardware stores state and changes it on defined events, usually clock edges.
Complete example	`A mux is combinational; a counter is sequential because it remembers its current count.`
Learner action	Which design requires stored state?
Expected knowledge	A counter
Teaching aid	COMBINATIONAL VERSUS SEQUENTIAL HARDWARE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify combinational versus sequential hardware
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Combinational versus sequential hardware

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 031 - 1.8 - Requirements become block diagrams

Theme and objective	A clear requirement is decomposed into inputs, outputs, state, datapaths, controls, clock/reset, and observable evidence before RTL is written.
Complete example	`A pulse counter requirement becomes synchronizer, edge detector, count register, display output, and reset blocks.`
Learner action	What should be identified before writing RTL?
Expected knowledge	Interfaces, state, timing, and required evidence
Teaching aid	REQUIREMENTS BECOME BLOCK DIAGRAMS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify requirements become block diagrams
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Requirements become block diagrams

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 032 - 1.9 - Read datasheets, guides, and schematics

Theme and objective	The device datasheet defines electrical and resource limits; the board guide and schematic define clocks, pins, peripherals, and board revisions.
Complete example	`A top-level LED port is assigned only after locating the LED net and FPGA package pin in the current schematic.`
Learner action	Which source is authoritative for a board LED pin?
Expected knowledge	The exact board revision schematic
Teaching aid	READ DATASHEETS, GUIDES, AND SCHEMATICS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify read datasheets, guides, and schematics
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Read datasheets, guides, and schematics

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 033 - 1.10 - First FPGA system review

Theme and objective	A complete introductory review connects requirements, resources, RTL, simulation, constraints, implementation, programming, and measured evidence.
Complete example	`Trace a switch-to-LED function from requirement through waveform and physical observation.`
Learner action	What makes the review complete?
Expected knowledge	Every stage is connected by repeatable evidence
Teaching aid	FIRST FPGA SYSTEM REVIEW - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify first fpga system review
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for First FPGA system review

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

2 - Read Verilog

Recognize the parts of a small hardware description.

Lesson 034 - 2.1 - Module, inputs, and outputs

Theme and objective	A module names one hardware block. Input ports bring signals into it. Output ports carry results out.
Complete example	`module and_gate(input a, input b, output y);`
Learner action	In the example, which name is the output signal?
Expected knowledge	y
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Module, inputs, and outputs
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 035 - 2.2 - Continuous assignment

Theme and objective	The assign keyword describes combinational hardware. The output changes whenever an input used by the expression changes.
Complete example	`assign y = a & b;`
Learner action	What circuit does the expression create?
Expected knowledge	An AND function
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Continuous assignment
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 036 - 2.3 - Operators you can see

Theme and objective	& means AND, | means OR, ^ means XOR, and ~ means NOT. These operators describe logic connections.
Complete example	`assign y = (a & b) | enable;`
Learner action	What makes y equal to 1 in this example?
Expected knowledge	enable is 1, or both a and b are 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Operators you can see
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 037 - 2.4 - logic, wire, and driven signals

Theme and objective	SystemVerilog logic represents a value driven by one intended source. Verilog wire represents a net connection. The declaration must match how the signal is driven.
Complete example	`logic y; always_comb y = a & b; wire z; assign z = y;`
Learner action	How many intended RTL drivers should a logic signal normally have?
Expected knowledge	One
Teaching aid	LOGIC, WIRE, AND DRIVEN SIGNALS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify logic, wire, and driven signals
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for logic, wire, and driven signals

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 038 - 2.5 - Vectors, indexing, and bit order

Theme and objective	Packed vectors group related bits. Declared bounds define legal indexes and must be followed consistently through ports and expressions.
Complete example	`logic [7:0] data; data[7] is the most-significant bit and data[0] is the least-significant bit.`
Learner action	Which slice selects the upper nibble?
Expected knowledge	data[7:4]
Teaching aid	VECTORS, INDEXING, AND BIT ORDER - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify vectors, indexing, and bit order
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Vectors, indexing, and bit order

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 039 - 2.6 - Expression width and precedence

Theme and objective	Operator precedence and expression width affect the synthesized result. Parentheses and explicit extensions make intent reviewable.
Complete example	`sum_ext = {1'b0,a} + {1'b0,b}; preserves the carry bit.`
Learner action	Why extend both operands before an addition?
Expected knowledge	To preserve the full-width result and carry
Teaching aid	EXPRESSION WIDTH AND PRECEDENCE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify expression width and precedence
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Expression width and precedence

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 040 - 2.7 - Named module instantiation

Theme and objective	A module instance creates reusable hardware. Named port connections make interfaces explicit and reduce errors caused by port ordering.
Complete example	`counter u_count(.clk(clk), .rst_n(rst_n), .count(count));`
Learner action	What is u_count?
Expected knowledge	One hardware instance of counter
Teaching aid	NAMED MODULE INSTANTIATION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify named module instantiation
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Named module instantiation

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 041 - 2.8 - Parameters and reusable widths

Theme and objective	Parameters configure constants such as bus width or depth at elaboration while retaining one verified module implementation.
Complete example	`fifo #(.DEPTH(16), .WIDTH(8)) u_fifo (...);`
Learner action	When are WIDTH and DEPTH used to create hardware?
Expected knowledge	During elaboration before synthesis
Teaching aid	PARAMETERS AND REUSABLE WIDTHS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify parameters and reusable widths
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Parameters and reusable widths

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 042 - 2.9 - Naming, polarity, and units

Theme and objective	Names should reveal purpose, polarity, clock domain, width, and units. Active-low signals are commonly marked with a suffix such as _n.
Complete example	`reset_n means reset is asserted at 0; timeout_cycles states both purpose and units.`
Learner action	What does the suffix _n normally communicate?
Expected knowledge	The signal is active-low
Teaching aid	NAMING, POLARITY, AND UNITS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify naming, polarity, and units
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Naming, polarity, and units

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 043 - 2.10 - Read an RTL subsystem capstone

Theme and objective	Reading RTL means tracing ports, parameters, combinational equations, clocked state, hierarchy, and reset behavior without assuming software execution order.
Complete example	`Trace valid and data through a parameterized register stage and state the edge on which output changes.`
Learner action	What should be traced first?
Expected knowledge	Ports, clocks, reset, and signal drivers
Teaching aid	READ AN RTL SUBSYSTEM CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify read an rtl subsystem capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Read an RTL subsystem capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

3 - Write and Simulate

Create a complete small design and prove its behavior.

Lesson 044 - 3.1 - Write the first module

Theme and objective	A complete module has a declaration, its logic, and endmodule.

Complete example	`module top(input a, b, output y);`
	`assign y = a & b;`
	`endmodule`

Learner action	Which line creates the actual logic?
Expected knowledge	assign y = a & b;
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Write the first module
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 045 - 3.2 - What a testbench does

Theme and objective	A testbench is simulation-only code. It drives inputs, waits, and checks outputs without becoming FPGA hardware.
Complete example	`Set a=1 and b=1; wait; check that y is 1.`
Learner action	Why test before programming the board?
Expected knowledge	To find behavior errors using repeatable input cases
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe What a testbench does
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 046 - 3.3 - Read a waveform

Theme and objective	A waveform plots signal values over time. Read inputs first, then compare the output at the same time.
Complete example	`When a=1 and b=1, an AND design must show y=1. For the other three input pairs, y=0.`
Learner action	For a=1 and b=0, what must y be?
Expected knowledge	0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Read a waveform
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 047 - 3.4 - Write complete combinational logic

Theme and objective	Combinational RTL assigns every output for every input case. Defaults followed by selected overrides prevent unintended storage.
Complete example	`always_comb begin y='0; if (enable) y=a; end`
Learner action	What happens if y has no assignment when enable is 0?
Expected knowledge	A latch may be inferred
Teaching aid	WRITE COMPLETE COMBINATIONAL LOGIC - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify write complete combinational logic
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Write complete combinational logic

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 048 - 3.5 - Exhaustive truth-table simulation

Theme and objective	Small combinational blocks can be tested exhaustively by applying every legal input combination and checking the exact output.
Complete example	`A two-input gate requires vectors 00, 01, 10, and 11.`
Learner action	How many vectors exhaustively test two binary inputs?
Expected knowledge	Four
Teaching aid	EXHAUSTIVE TRUTH-TABLE SIMULATION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify exhaustive truth-table simulation
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Exhaustive truth-table simulation

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 049 - 3.6 - Clocked testbench stimulus

Theme and objective	Sequential testbenches drive reset and data away from the sampling edge, then check outputs after the specified edge and settling interval.
Complete example	`Drive D before posedge clk; sample Q just after posedge clk.`
Learner action	When must D be valid for a rising-edge register test?
Expected knowledge	Before the rising edge
Teaching aid	CLOCKED TESTBENCH STIMULUS - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify clocked testbench stimulus
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Clocked testbench stimulus

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 050 - 3.7 - Self-checking tests and failures

Theme and objective	A self-checking test computes or stores the expected result, compares it with the DUT, and reports enough context to reproduce a failure.
Complete example	`if (actual !== expected) $fatal("vector=%h", vector);`
Learner action	What must a useful failure report identify?
Expected knowledge	Stimulus, expected value, and observed value
Teaching aid	SELF-CHECKING TESTS AND FAILURES - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify self-checking tests and failures
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Self-checking tests and failures

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 051 - 3.8 - Diagnose X, Z, and contention

Theme and objective	X indicates unknown or conflicting state; Z indicates high impedance. Both require tracing initialization, enable, and every active driver.
Complete example	`Two drivers forcing different values resolve to X; no enabled driver resolves to Z.`
Learner action	What does Z usually mean?
Expected knowledge	No active driver controls the net
Teaching aid	DIAGNOSE X, Z, AND CONTENTION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify diagnose x, z, and contention
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Diagnose X, Z, and contention

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 052 - 3.9 - Regression tests and recorded seeds

Theme and objective	A regression reruns a stable set of tests after each design change. Randomized tests record their seed so every failure can be reproduced.
Complete example	`Run directed reset tests plus 100 randomized transactions and archive seed 4721.`
Learner action	Why record the random seed?
Expected knowledge	To reproduce the same stimulus sequence
Teaching aid	REGRESSION TESTS AND RECORDED SEEDS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify regression tests and recorded seeds
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Regression tests and recorded seeds

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 053 - 3.10 - First verified subsystem

Theme and objective	A verified subsystem has a written interface contract, synthesizable RTL, repeatable tests, explained coverage, and a clean result for boundary cases.
Complete example	`Deliver a mux/register block with reset, enable, exhaustive control tests, and waveform evidence.`
Learner action	What is required in addition to a passing example?
Expected knowledge	Boundary tests and reproducible checks
Teaching aid	FIRST VERIFIED SUBSYSTEM - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify first verified subsystem
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for First verified subsystem

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

4 - Build Clocked RTL

Understand registers, clocks, reset, and state.

Lesson 054 - 4.1 - The clock edge

Theme and objective	A register samples its input at a chosen clock edge and holds that value between edges.
Complete example	`always_ff @(posedge clk) q <= d;`
Learner action	When does q copy d?
Expected knowledge	At the rising edge of clk
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe The clock edge
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 055 - 4.2 - Reset gives a known start

Theme and objective	Reset places stored state into a defined value so the circuit does not begin unpredictably.
Complete example	`if (!rst_n) q <= 0; else q <= d;`
Learner action	What value is loaded while rst_n is low?
Expected knowledge	0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Reset gives a known start
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: CLK, RST, Q	Interactive inputs: RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 056 - 4.3 - Build a counter

Theme and objective	A counter is a register whose next value is its current value plus one.
Complete example	`count <= count + 1;`
Learner action	If count is 7 before the clock edge, what is it after the edge?
Expected knowledge	8
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Build a counter
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 057 - 4.4 - Register enable and hold behavior

Theme and objective	A register enable updates state only on selected clock edges. When enable is low, state retains its previous value.
Complete example	`if (enable) q <= d; leaves q unchanged when enable=0.`
Learner action	What does q do on an edge with enable=0?
Expected knowledge	It holds its previous value
Teaching aid	REGISTER ENABLE AND HOLD BEHAVIOR - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify register enable and hold behavior
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Register enable and hold behavior

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 058 - 4.5 - Synchronous versus asynchronous reset

Theme and objective	Synchronous reset is sampled by the clock. Asynchronous reset asserts without waiting for an edge and requires controlled deassertion.
Complete example	`always_ff @(posedge clk or negedge rst_n) describes asynchronous assertion.`
Learner action	Which transition requires special synchronization?
Expected knowledge	Asynchronous reset deassertion
Teaching aid	SYNCHRONOUS VERSUS ASYNCHRONOUS RESET - ASYNC_IN -> SYNC1 -> SYNC2 -> EVENT annotated concept and waveform view
Lab target	implement, predict, and verify synchronous versus asynchronous reset
Controls / actions	ten progressive activities using ASYNC_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Synchronous versus asynchronous reset

Signals: CLK, ASYNC_IN, SYNC1, SYNC2, EVENT	Interactive inputs: ASYNC_IN, RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 059 - 4.6 - Shift register data movement

Theme and objective	A shift register moves stored bits one position per enabled clock edge and is used for delay, serialization, and history.
Complete example	`q <= {q[6:0], serial_in}; shifts one new bit into q[0].`
Learner action	How many enabled edges move a bit across an 8-stage register?
Expected knowledge	Eight
Teaching aid	SHIFT REGISTER DATA MOVEMENT - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify shift register data movement
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Shift register data movement

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 060 - 4.7 - Counter width and rollover

Theme and objective	An N-bit counter represents 0 through 2^N-1 and wraps unless terminal-count logic changes its sequence.
Complete example	`A 4-bit counter advances from 15 to 0.`
Learner action	What follows 255 in an 8-bit free-running counter?
Expected knowledge	0
Teaching aid	COUNTER WIDTH AND ROLLOVER - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify counter width and rollover
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Counter width and rollover

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 061 - 4.8 - FSM state and next-state logic

Theme and objective	A finite-state machine separates the current-state register from next-state decisions and defined outputs.
Complete example	`IDLE waits for start; RUN counts; DONE asserts valid until acknowledged.`
Learner action	Which block stores the active FSM state?
Expected knowledge	The state register
Teaching aid	FSM STATE AND NEXT-STATE LOGIC - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify fsm state and next-state logic
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for FSM state and next-state logic

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 062 - 4.9 - Synchronize external control inputs

Theme and objective	Buttons and external controls are asynchronous to the FPGA clock. A synchronizer reduces metastability propagation before edge detection or control logic.
Complete example	`button -> synchronizer FF1 -> FF2 -> edge detector.`
Learner action	Why not feed a raw button directly to many registers?
Expected knowledge	It can violate sampling timing and propagate metastability
Teaching aid	SYNCHRONIZE EXTERNAL CONTROL INPUTS - ASYNC_IN -> SYNC1 -> SYNC2 -> EVENT annotated concept and waveform view
Lab target	implement, predict, and verify synchronize external control inputs
Controls / actions	ten progressive activities using ASYNC_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Synchronize external control inputs

Signals: CLK, ASYNC_IN, SYNC1, SYNC2, EVENT	Interactive inputs: ASYNC_IN
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 063 - 4.10 - Clocked controller capstone

Theme and objective	A robust controller combines synchronized inputs, defined reset, state transitions, counters, enables, and observable outputs.
Complete example	`A start button launches a timed sequence, ignores repeated starts while busy, and asserts done for one cycle.`
Learner action	What must verification prove about start while busy?
Expected knowledge	It follows the documented ignore or queue policy
Teaching aid	CLOCKED CONTROLLER CAPSTONE - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify clocked controller capstone
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Clocked controller capstone

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

5 - Map RTL into an FPGA

Connect HDL concepts to physical FPGA resources.

Lesson 064 - 5.1 - Synthesis

Theme and objective	Synthesis translates synthesizable Verilog into a network of logic resources and registers.
Complete example	`assign y=a&b normally maps into a lookup table; a clocked q normally maps into a flip-flop.`
Learner action	Which result belongs to synthesis?
Expected knowledge	A logic netlist made from FPGA resources
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Synthesis
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 065 - 5.2 - Place and route

Theme and objective	Placement chooses physical resources. Routing connects those resources using programmable wires.
Complete example	`The tool places a LUT and output cell, then routes the LUT result to that cell.`
Learner action	What does routing create?
Expected knowledge	Connections between placed resources
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Place and route
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 066 - 5.3 - Timing must pass

Theme and objective	Timing analysis checks whether data can travel and settle before the next required clock edge.
Complete example	`A 10 ns clock period requires the relevant path to complete within its available time.`
Learner action	What does a timing failure mean?
Expected knowledge	A path may not deliver stable data in time
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Timing must pass
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 067 - 5.4 - Lookup tables implement equations

Theme and objective	A LUT stores the truth table of a small Boolean function. Synthesis maps equivalent RTL expressions into available LUT resources.
Complete example	`A four-input Boolean equation can be represented by sixteen LUT truth values.`
Learner action	What does a LUT fundamentally store?
Expected knowledge	A truth table
Teaching aid	LOOKUP TABLES IMPLEMENT EQUATIONS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify lookup tables implement equations
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Lookup tables implement equations

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 068 - 5.5 - Flip-flop packing and enables

Theme and objective	FPGA logic elements commonly pair a LUT with a flip-flop and supported enable/reset controls. RTL style affects packing and routing.
Complete example	`A registered LUT result can use neighboring fabric resources with short routing.`
Learner action	Why register a long combinational result?
Expected knowledge	To create a timed pipeline boundary
Teaching aid	FLIP-FLOP PACKING AND ENABLES - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify flip-flop packing and enables
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Flip-flop packing and enables

Signals: CLK, STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 069 - 5.6 - Carry chains and DSP arithmetic

Theme and objective	Dedicated carry and DSP resources implement arithmetic more efficiently than arbitrary fabric routing when RTL matches supported structures.
Complete example	`A wide adder uses a carry chain; a multiply-accumulate can use a DSP block.`
Learner action	Which resource best fits repeated multiply-accumulate?
Expected knowledge	A DSP block
Teaching aid	CARRY CHAINS AND DSP ARITHMETIC - A -> B -> RESULT -> VALID -> OVERFLOW annotated concept and waveform view
Lab target	implement, predict, and verify carry chains and dsp arithmetic
Controls / actions	ten progressive activities using A, B
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Carry chains and DSP arithmetic

Signals: A, B, RESULT, VALID, OVERFLOW	Interactive inputs: A, B
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 070 - 5.7 - Embedded memory mapping

Theme and objective	Arrays with supported synchronous access patterns map to embedded memory; unsupported patterns may consume excessive LUT fabric.
Complete example	`A synchronous single-write-port array can infer block RAM.`
Learner action	What should be checked after synthesis?
Expected knowledge	The intended embedded memory was inferred
Teaching aid	EMBEDDED MEMORY MAPPING - ADDRESS -> WRITE -> DATA_IN -> DATA_OUT -> VALID annotated concept and waveform view
Lab target	implement, predict, and verify embedded memory mapping
Controls / actions	ten progressive activities using ADDRESS, WRITE, DATA_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Embedded memory mapping

Signals: ADDRESS, WRITE, DATA_IN, DATA_OUT, VALID	Interactive inputs: ADDRESS, WRITE, DATA_IN
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data transcript, boundary cases, and pass LED

Lesson 071 - 5.8 - Global clock networks

Theme and objective	Dedicated clock networks distribute supported clocks with controlled skew. Fabric logic should not casually create or gate clocks.
Complete example	`Use a clock enable instead of clk & enable as a new fabric clock.`
Learner action	What is the preferred way to pause state updates?
Expected knowledge	Use a register clock enable
Teaching aid	GLOBAL CLOCK NETWORKS - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify global clock networks
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Global clock networks

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 072 - 5.9 - I/O cells, banks, and voltage

Theme and objective	Package pins belong to I/O banks with voltage and standard restrictions. Pin selection must satisfy the board connection and bank electrical rules.
Complete example	`An LVCMOS port uses a compatible bank voltage and documented board net.`
Learner action	What must be checked before assigning an I/O standard?
Expected knowledge	Bank voltage and board electrical requirements
Teaching aid	I/O CELLS, BANKS, AND VOLTAGE - INPUT_PIN -> INTERNAL -> OUTPUT_PIN -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify i/o cells, banks, and voltage
Controls / actions	ten progressive activities using INPUT_PIN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for I/O cells, banks, and voltage

Signals: INPUT_PIN, INTERNAL, OUTPUT_PIN, OBSERVED	Interactive inputs: INPUT_PIN
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 073 - 5.10 - Resource and timing mapping capstone

Theme and objective	A mapping review connects each RTL structure to inferred resources, placement, routing, utilization, clocks, and critical timing paths.
Complete example	`Explain why a counter uses flip-flops and carry logic while its status flag uses LUT logic.`
Learner action	What validates a mapping claim?
Expected knowledge	Synthesis and implementation reports
Teaching aid	RESOURCE AND TIMING MAPPING CAPSTONE - INPUT_PIN -> INTERNAL -> OUTPUT_PIN -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify resource and timing mapping capstone
Controls / actions	ten progressive activities using INPUT_PIN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Resource and timing mapping capstone

Signals: INPUT_PIN, INTERNAL, OUTPUT_PIN, OBSERVED	Interactive inputs: INPUT_PIN
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

6 - Put It on the PolarFire Board

Complete the real Libero-to-board workflow.

Lesson 074 - 6.1 - Create the Libero project

Theme and objective	The project records the target FPGA family, device, package, HDL sources, constraints, and tool results.
Complete example	`Choose the device used by the PolarFire SoC Discovery Kit, add the top-level Verilog module, and build hierarchy.`
Learner action	Why must the exact device and package be selected?
Expected knowledge	Resources and physical pins depend on the selected device
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Create the Libero project
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 075 - 6.2 - Assign board pins

Theme and objective	A top-level port must be constrained to the physical pin wired to the intended switch, button, clock, or LED.
Complete example	`The port led must use the board pin connected to the chosen LED, with the correct I/O standard.`
Learner action	What happens if led is assigned to the wrong pin?
Expected knowledge	The intended board LED will not receive that signal
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Assign board pins
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 076 - 6.3 - Program and verify

Theme and objective	After synthesis, place-and-route, and timing checks, generate the programming image, program the FPGA, then exercise the real inputs and observe outputs.
Complete example	`Press the assigned switch and confirm the assigned LED follows the behavior already proven in simulation.`
Learner action	What is the strongest completion evidence?
Expected knowledge	Simulation passes, timing passes, and the board matches the test plan
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Program and verify
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 077 - 6.4 - Constrain the board clock and reset

Theme and objective	The physical oscillator pin, clock period, reset pin, polarity, and I/O standard must match the exact board documentation.
Complete example	`A verified 100 MHz source receives a 10 ns create_clock constraint.`
Learner action	What must be verified before using a 10 ns period?
Expected knowledge	The selected board clock is 100 MHz
Teaching aid	CONSTRAIN THE BOARD CLOCK AND RESET - RST -> D -> Q annotated concept and waveform view
Lab target	implement, predict, and verify constrain the board clock and reset
Controls / actions	ten progressive activities using D
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Constrain the board clock and reset

Signals: CLK, RST, D, Q	Interactive inputs: D, RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 078 - 6.5 - Switch, button, and LED top level

Theme and objective	The board top module connects physical switches and buttons to synchronized internal logic and drives documented LED outputs.
Complete example	`switch[0] selects a mode; button[0] creates a debounced start; led[0] shows done.`
Learner action	Which input normally needs synchronization and debounce?
Expected knowledge	A mechanical push button
Teaching aid	SWITCH, BUTTON, AND LED TOP LEVEL - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify switch, button, and led top level
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Switch, button, and LED top level

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 079 - 6.6 - Simulate the complete board top

Theme and objective	Simulation must include the top-level wrapper, reset sequence, clock, physical input conventions, and expected output polarity before implementation.
Complete example	`The testbench models an active-low button and verifies the visible LED convention.`
Learner action	Why simulate the wrapper instead of only the core?
Expected knowledge	To verify integration, polarity, and port behavior
Teaching aid	SIMULATE THE COMPLETE BOARD TOP - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify simulate the complete board top
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Simulate the complete board top

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 080 - 6.7 - Review implementation reports

Theme and objective	A completed implementation review checks hierarchy, inferred resources, clocks, unconstrained paths, warnings, utilization, and setup/hold timing.
Complete example	`Every warning receives a written disposition before programming data is accepted.`
Learner action	What makes a warning acceptable?
Expected knowledge	Its cause and impact are understood and documented
Teaching aid	REVIEW IMPLEMENTATION REPORTS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify review implementation reports
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Review implementation reports

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 081 - 6.8 - Programming image and safe handling

Theme and objective	Programming occurs only after the correct device, constraints, timing, and board power/programmer connections are verified.
Complete example	`Record the programming-image digest, tool version, device, board revision, and result.`
Learner action	What prevents programming the wrong project by mistake?
Expected knowledge	A traceable image and target checklist
Teaching aid	PROGRAMMING IMAGE AND SAFE HANDLING - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify programming image and safe handling
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Programming image and safe handling

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 082 - 6.9 - Collect repeatable board evidence

Theme and objective	Board evidence records exact stimulus, expected behavior, observed result, timing, environment, and any measurement instrument settings.
Complete example	`Apply switch vectors 00, 01, 10, 11 and record LED output beside simulation predictions.`
Learner action	What makes a photograph useful evidence?
Expected knowledge	It is labeled and tied to a documented stimulus
Teaching aid	COLLECT REPEATABLE BOARD EVIDENCE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify collect repeatable board evidence
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Collect repeatable board evidence

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 083 - 6.10 - PolarFire board bring-up capstone

Theme and objective	Bring-up proceeds from power and programmer detection through clock/reset, one known I/O path, full stimulus, and archived results.
Complete example	`First prove a heartbeat LED, then test the lesson datapath, then compare every case with simulation.`
Learner action	What should be tested first on an unknown board state?
Expected knowledge	A minimal known clock/reset and I/O path
Teaching aid	POLARFIRE BOARD BRING-UP CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify polarfire board bring-up capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for PolarFire board bring-up capstone

Signals: CLK, STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS, RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

7 - Combinational Verilog

Write reusable combinational RTL without accidental storage.

Lesson 084 - 7.1 - Vectors and slices

Theme and objective	Packed vectors group related bits into buses. A slice selects a defined range without changing hardware time.
Complete example	`logic [7:0] data; assign low = data[3:0];`
Learner action	Which expression selects the upper nibble?
Expected knowledge	data[7:4]
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Vectors and slices
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 085 - 7.2 - always_comb blocks

Theme and objective	always_comb describes combinational decisions and requires every assigned output to receive a value on every path.
Complete example	`always_comb begin y = 0; if (en) y = a; end`
Learner action	Why is y assigned before the if?
Expected knowledge	To provide a default and avoid a latch
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe always_comb blocks
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 086 - 7.3 - case and priority

Theme and objective	case expresses mutually selected alternatives. priority and unique intent should match the real input rules.
Complete example	`case (sel) 2'b00:y=a; 2'b01:y=b; default:y=0; endcase`
Learner action	What prevents an uncovered selection?
Expected knowledge	A default assignment
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe case and priority
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 087 - 7.4 - Parameters and widths

Theme and objective	Parameters make module widths configurable while keeping one verified implementation.
Complete example	`module add #(parameter W=8)(input logic [W-1:0] a,b);`
Learner action	What does W control?
Expected knowledge	The bus width
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Parameters and widths
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 088 - 7.5 - Module hierarchy

Theme and objective	Larger designs instantiate verified modules and connect them using explicit named ports.
Complete example	`adder u_add(.a(a), .b(b), .y(sum));`
Learner action	What is u_add?
Expected knowledge	An instance of adder
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Module hierarchy
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 089 - 7.6 - Priority encoder RTL

Theme and objective	A priority encoder defines which active input wins and reports whether any valid input exists.
Complete example	`If requests 7 and 3 are both high, the documented highest-priority request 7 is encoded.`
Learner action	What must the RTL define for simultaneous requests?
Expected knowledge	A deterministic priority rule
Teaching aid	PRIORITY ENCODER RTL - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify priority encoder rtl
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Priority encoder RTL

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 090 - 7.7 - Comparators and range checks

Theme and objective	Equality, magnitude, and range comparisons are combinational functions whose signedness and width must be explicit.
Complete example	`inside = (value >= low) && (value <= high);`
Learner action	What can change a magnitude comparison result?
Expected knowledge	Signed versus unsigned interpretation
Teaching aid	COMPARATORS AND RANGE CHECKS - A -> B -> RESULT -> VALID -> OVERFLOW annotated concept and waveform view
Lab target	implement, predict, and verify comparators and range checks
Controls / actions	ten progressive activities using A, B
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Comparators and range checks

Signals: A, B, RESULT, VALID, OVERFLOW	Interactive inputs: A, B
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 091 - 7.8 - Decoder and mux structures

Theme and objective	Decoders create one-hot control, while multiplexers select one data source. Defaults define inactive and illegal selections.
Complete example	`A decoded write enable selects one register; a mux returns the selected register value.`
Learner action	Why include a default output?
Expected knowledge	To define every combinational input case
Teaching aid	DECODER AND MUX STRUCTURES - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify decoder and mux structures
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Decoder and mux structures

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 092 - 7.9 - Parameterized adder with carry

Theme and objective	A reusable adder explicitly extends operands so the carry bit is preserved for any supported width.
Complete example	`logic [W:0] sum_ext = {1'b0,a}+{1'b0,b};`
Learner action	How wide is sum_ext for W-bit operands?
Expected knowledge	W+1 bits
Teaching aid	PARAMETERIZED ADDER WITH CARRY - A -> B -> RESULT -> VALID -> OVERFLOW annotated concept and waveform view
Lab target	implement, predict, and verify parameterized adder with carry
Controls / actions	ten progressive activities using A, B
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Parameterized adder with carry

Signals: A, B, RESULT, VALID, OVERFLOW	Interactive inputs: A, B
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 093 - 7.10 - Combinational datapath capstone

Theme and objective	A combinational datapath integrates decode, arithmetic, comparison, selection, status, defaults, and exhaustive verification without latches.
Complete example	`An operation code selects add, mask, compare, or pass-through and reports carry/zero.`
Learner action	What proves no selection case is missing?
Expected knowledge	Defaults plus complete checking of legal and illegal controls
Teaching aid	COMBINATIONAL DATAPATH CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify combinational datapath capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Combinational datapath capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

8 - Sequential RTL

Design deterministic state, counters, enables, and finite-state machines.

Lesson 094 - 8.1 - Nonblocking assignments

Theme and objective	Clocked RTL uses nonblocking assignments so all registers observe the pre-edge state together.
Complete example	`always_ff @(posedge clk) q <= d;`
Learner action	Which assignment belongs in clocked RTL?
Expected knowledge	<=
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Nonblocking assignments
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 095 - 8.2 - Clock enable

Theme and objective	A clock enable updates state only on selected edges while using the FPGA clock network normally.
Complete example	`if (enable) q <= d;`
Learner action	What happens when enable is 0?
Expected knowledge	q holds its previous value
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Clock enable
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 096 - 8.3 - Synchronous and asynchronous reset

Theme and objective	A synchronous reset is sampled at the clock edge; an asynchronous reset can affect state without waiting for an edge.
Complete example	`always_ff @(posedge clk or negedge rst_n)`
Learner action	Which signal acts asynchronously here?
Expected knowledge	rst_n
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Synchronous and asynchronous reset
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: CLK, RST, Q	Interactive inputs: RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 097 - 8.4 - Counters and rollover

Theme and objective	An N-bit counter wraps modulo 2^N unless extra range logic changes that behavior.
Complete example	`logic [3:0] count; count <= count + 1'b1;`
Learner action	What follows 15?
Expected knowledge	0
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Counters and rollover
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 098 - 8.5 - Finite-state machines

Theme and objective	An FSM separates stored state, next-state decisions, and outputs so transitions can be reviewed and verified.
Complete example	`IDLE -> LOAD -> RUN -> DONE`
Learner action	Which block stores the current state?
Expected knowledge	A state register
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Finite-state machines
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, INPUT, STATE, OUTPUT	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 099 - 8.6 - Serial and parallel shift registers

Theme and objective	Shift registers convert serial and parallel data and provide precisely counted cycle delays.
Complete example	`Eight enabled edges load one serial byte into an 8-bit register.`
Learner action	What determines the output timing?
Expected knowledge	Clock edges and enable behavior
Teaching aid	SERIAL AND PARALLEL SHIFT REGISTERS - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify serial and parallel shift registers
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Serial and parallel shift registers

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 100 - 8.7 - Edge and pulse counters

Theme and objective	A pulse counter detects qualified events, increments once per event, and defines overflow and clear behavior.
Complete example	`Synchronize an input, detect its rising edge, then increment count.`
Learner action	Why detect an edge instead of counting high cycles?
Expected knowledge	To count one event per transition
Teaching aid	EDGE AND PULSE COUNTERS - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify edge and pulse counters
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Edge and pulse counters

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 101 - 8.8 - Timers and PWM state

Theme and objective	Timers count clock intervals; PWM compares a running counter with duty. Width and terminal values define the period.
Complete example	`An 8-bit PWM counter creates 256 time steps per period.`
Learner action	What changes PWM average high time?
Expected knowledge	The duty compare value
Teaching aid	TIMERS AND PWM STATE - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify timers and pwm state
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Timers and PWM state

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 102 - 8.9 - Safe FSM outputs and recovery

Theme and objective	FSM outputs are defined in every state, illegal encodings recover safely, and transition conditions are mutually reviewable.
Complete example	`default: next_state=IDLE; outputs=0;` prevents uncontrolled illegal-state behavior.
Learner action	What should an illegal state do?
Expected knowledge	Recover according to the documented safe policy
Teaching aid	SAFE FSM OUTPUTS AND RECOVERY - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify safe fsm outputs and recovery
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Safe FSM outputs and recovery

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 103 - 8.10 - Sequential controller capstone

Theme and objective	A sequential capstone combines synchronized commands, timer/counter state, enable, reset, FSM control, status, and self-checking sequences.
Complete example	`A transaction controller accepts start, runs for N cycles, produces valid, and waits for acknowledgement.`
Learner action	What prevents a new start from corrupting an active transaction?
Expected knowledge	A defined busy/start acceptance rule
Teaching aid	SEQUENTIAL CONTROLLER CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify sequential controller capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Sequential controller capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

9 - Verification Engineering

Build self-checking simulations that detect errors automatically.

Lesson 104 - 9.1 - Clock and reset generation

Theme and objective	A testbench provides repeatable clock and reset stimulus before functional vectors begin.
Complete example	`initial clk=0; always #5 clk=~clk;`
Learner action	What period does this clock have?
Expected knowledge	10 time units
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Clock and reset generation
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, RST, Q	Interactive inputs: RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 105 - 9.2 - Reusable stimulus tasks

Theme and objective	Tasks package repeated bus operations while keeping timing and protocol rules in one place.
Complete example	`task send_byte(input [7:0] value);`
Learner action	Why use a task?
Expected knowledge	To reuse a verified stimulus sequence
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Reusable stimulus tasks
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 106 - 9.3 - Scoreboards

Theme and objective	A scoreboard computes or stores expected results and compares them with actual DUT outputs.
Complete example	`if (actual !== expected) $error;`
Learner action	What does the scoreboard detect?
Expected knowledge	A functional mismatch
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Scoreboards
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, CHECK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 107 - 9.4 - Assertions

Theme and objective	Assertions state temporal rules such as request eventually receiving acknowledgement or reset clearing state.
Complete example	`assert property (@(posedge clk) req |-> ##[1:3] ack);`
Learner action	What is being bounded?
Expected knowledge	The allowed acknowledgement latency
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Assertions
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, CHECK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 108 - 9.5 - Functional coverage

Theme and objective	Coverage records which meaningful scenarios occurred and reveals untested combinations.
Complete example	`covergroup inputs; coverpoint opcode; endgroup`
Learner action	What does a coverage hole mean?
Expected knowledge	A required scenario was not exercised
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Functional coverage
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, CHECK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 109 - 9.6 - Directed and constrained-random stimulus

Theme and objective	Directed cases guarantee critical boundaries; constrained-random cases explore legal combinations not anticipated manually.
Complete example	`Always test reset and overflow directly, then randomize legal transactions with a recorded seed.`
Learner action	Why use both stimulus styles?
Expected knowledge	They combine guaranteed coverage with broader exploration
Teaching aid	DIRECTED AND CONSTRAINED-RANDOM STIMULUS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify directed and constrained-random stimulus
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Directed and constrained-random stimulus

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 110 - 9.7 - Immediate and temporal assertions

Theme and objective	Immediate assertions check current expressions; temporal assertions check relationships across clock cycles.
Complete example	`req |-> ##[1:3] ack requires acknowledgement one to three cycles later.`
Learner action	What does the range [1:3] define?
Expected knowledge	Allowed acknowledgement latency
Teaching aid	IMMEDIATE AND TEMPORAL ASSERTIONS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify immediate and temporal assertions
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Immediate and temporal assertions

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 111 - 9.8 - Coverage models and closure

Theme and objective	Coverage models record required states, transitions, values, and crosses. Closure requires explaining or exercising every meaningful hole.
Complete example	`Cross operation with overflow to ensure each operation is tested at the boundary.`
Learner action	What is a coverage hole?
Expected knowledge	A required scenario not yet observed
Teaching aid	COVERAGE MODELS AND CLOSURE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify coverage models and closure
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Coverage models and closure

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 112 - 9.9 - Reference models and scoreboards

Theme and objective	A reference model independently predicts results. A scoreboard aligns transactions and compares expected with observed output.
Complete example	`Queue expected ALU responses, then compare each DUT valid response in order.`
Learner action	Why keep the predictor independent from DUT RTL?
Expected knowledge	To avoid reproducing the same implementation error
Teaching aid	REFERENCE MODELS AND SCOREBOARDS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify reference models and scoreboards
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Reference models and scoreboards

Signals: CLK, VALID, READY, EXPECTED, ACTUAL, MATCH, STIMULUS, OBSERVED	Interactive inputs: VALID, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 113 - 9.10 - Verification regression capstone

Theme and objective	A regression capstone runs lint/validation, directed tests, seeded random tests, assertions, coverage, and summarized failures automatically.
Complete example	`One command records tool version, seed, tests, assertion failures, and coverage report.`
Learner action	What makes the regression trustworthy?
Expected knowledge	Repeatable inputs, automatic checks, and archived results
Teaching aid	VERIFICATION REGRESSION CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify verification regression capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Verification regression capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

10 - Pipelines, Handshakes, and CDC

Move data safely through high-performance and multi-clock systems.

Lesson 114 - 10.1 - Pipeline registers

Theme and objective	Pipelining divides a long combinational path across cycles to improve achievable clock frequency.
Complete example	`stage1 <= a*b; stage2 <= stage1+c;`
Learner action	What tradeoff is added?
Expected knowledge	More latency
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Pipeline registers
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 115 - 10.2 - Valid and ready handshake

Theme and objective	A transfer occurs only when valid and ready are both asserted on the sampling edge.
Complete example	`transfer = valid && ready;`
Learner action	When does data move?
Expected knowledge	When valid and ready are both 1
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Valid and ready handshake
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: VALID, READY, TRANSFER	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 116 - 10.3 - FIFO buffering

Theme and objective	A FIFO absorbs rate differences while preserving ordering and reporting full and empty status.
Complete example	`write pointer, read pointer, memory`
Learner action	Which item leaves first?
Expected knowledge	The earliest item written
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe FIFO buffering
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, WRITE, READ, LEVEL	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data reported over UART with a pass/fail LED

Lesson 117 - 10.4 - Metastability

Theme and objective	An asynchronous transition near a sampling edge can violate setup or hold and place a flip-flop in a metastable state.
Complete example	`async input -> synchronizer FF1 -> FF2`
Learner action	What reduces propagation risk for a single bit?
Expected knowledge	A two-flop synchronizer
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Metastability
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 118 - 10.5 - Clock-domain crossing protocols

Theme and objective	Multi-bit data requires a handshake, Gray code, or asynchronous FIFO rather than independent bit synchronizers.
Complete example	`Gray-coded FIFO pointers cross domains`
Learner action	Why use Gray code for a pointer?
Expected knowledge	Only one pointer bit changes per step
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Clock-domain crossing protocols
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 119 - 10.6 - Skid buffers under backpressure

Theme and objective	A skid buffer holds one transfer when ready falls late, preserving data and valid without duplication or loss.
Complete example	`If valid=1 and ready changes to 0, the offered data is captured until transfer resumes.`
Learner action	What must remain stable while valid=1 and ready=0?
Expected knowledge	The offered data and valid state
Teaching aid	SKID BUFFERS UNDER BACKPRESSURE - VALID -> READY -> DATA -> TRANSFER annotated concept and waveform view
Lab target	implement, predict, and verify skid buffers under backpressure
Controls / actions	ten progressive activities using VALID, READY, DATA
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Skid buffers under backpressure

Signals: VALID, READY, DATA, TRANSFER	Interactive inputs: VALID, READY, DATA
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 120 - 10.7 - Pulse and toggle CDC transfer

Theme and objective	A narrow pulse can disappear between unrelated clocks. Pulse stretching, toggles, or handshakes preserve the event until observed.
Complete example	`Source toggles a bit per event; destination synchronizes it and detects a change.`
Learner action	Why is a raw one-cycle pulse unsafe across domains?
Expected knowledge	The destination may never sample it
Teaching aid	PULSE AND TOGGLE CDC TRANSFER - ASYNC_IN -> SYNC1 -> SYNC2 -> EVENT annotated concept and waveform view
Lab target	implement, predict, and verify pulse and toggle cdc transfer
Controls / actions	ten progressive activities using ASYNC_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Pulse and toggle CDC transfer

Signals: CLK, ASYNC_IN, SYNC1, SYNC2, EVENT	Interactive inputs: ASYNC_IN
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 121 - 10.8 - Reset-domain crossing

Theme and objective	Reset assertion and deassertion affect domain state and interfaces. Deassertion is synchronized per clock domain before normal transfers begin.
Complete example	`Each domain uses a reset synchronizer and asserts ready only after local release.`
Learner action	What can unsynchronized reset release cause?
Expected knowledge	Different registers may resume on inconsistent edges
Teaching aid	RESET-DOMAIN CROSSING - RST -> D -> Q annotated concept and waveform view
Lab target	implement, predict, and verify reset-domain crossing
Controls / actions	ten progressive activities using D
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Reset-domain crossing

Signals: CLK, RST, D, Q	Interactive inputs: D, RST
In-app controls: clocked, resettable	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 122 - 10.9 - Measure latency and throughput

Theme and objective	Latency counts time or cycles from acceptance to response; throughput counts completed transfers per interval after pipeline fill.
Complete example	`A four-stage pipeline has four-cycle latency but can sustain one result each cycle.`
Learner action	Can high throughput coexist with multi-cycle latency?
Expected knowledge	Yes, when pipeline stages overlap transactions
Teaching aid	MEASURE LATENCY AND THROUGHPUT - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify measure latency and throughput
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Measure latency and throughput

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 123 - 10.10 - Streaming pipeline capstone

Theme and objective	A complete streaming design combines pipelined processing, valid/ready, backpressure, buffering, reset, and CDC boundaries with no loss or reordering.
Complete example	`Random stalls exercise a processing pipeline while a scoreboard verifies ordered outputs.`
Learner action	What must be proven during backpressure?
Expected knowledge	No accepted item is lost, duplicated, or reordered
Teaching aid	STREAMING PIPELINE CAPSTONE - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify streaming pipeline capstone
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Streaming pipeline capstone

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

11 - Memories and DSP

Use FPGA memory blocks and arithmetic resources effectively.

Lesson 124 - 11.1 - ROM inference

Theme and objective	A constant lookup table can infer ROM and provides deterministic mapped values.
Complete example	`case(address) 0:data=8'h3C; endcase`
Learner action	What selects the stored value?
Expected knowledge	The address
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe ROM inference
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: ADDRESS, DATA, VALID	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data reported over UART with a pass/fail LED

Lesson 125 - 11.2 - Block RAM inference

Theme and objective	Synchronous array templates map large storage into dedicated FPGA RAM instead of LUTs.
Complete example	`always_ff @(posedge clk) if (we) mem[addr] <= din;`
Learner action	When is a write performed?
Expected knowledge	On a clock edge with we asserted
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Block RAM inference
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, ADDRESS, DATA, VALID	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data reported over UART with a pass/fail LED

Lesson 126 - 11.3 - Dual-port memory

Theme and objective	Dual-port RAM supports two controlled accesses and requires explicit collision behavior.
Complete example	`port A writes while port B reads`
Learner action	What must be defined for one-address collisions?
Expected knowledge	Read/write collision behavior
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Dual-port memory
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, ADDRESS, DATA, VALID	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data reported over UART with a pass/fail LED

Lesson 127 - 11.4 - DSP multiply-accumulate

Theme and objective	Dedicated DSP blocks efficiently implement multiplication, addition, and accumulation pipelines.
Complete example	`acc <= acc + a*b;`
Learner action	Which FPGA resource best matches this operation?
Expected knowledge	A DSP block
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe DSP multiply-accumulate
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 128 - 11.5 - Fixed-point arithmetic

Theme and objective	Fixed-point values assign an implied binary point and require planned width, rounding, saturation, and overflow handling.
Complete example	`Q1.7 uses one integer/sign region and seven fractional bits`
Learner action	What must remain consistent?
Expected knowledge	The binary-point position
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Fixed-point arithmetic
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 129 - 11.6 - ROM initialization and lookup tables

Theme and objective	ROM contents can be defined by constants or supported initialization files. Address range and read latency are part of the interface.
Complete example	`A sine table maps phase address to a fixed amplitude sample.`
Learner action	What must simulation and hardware share?
Expected knowledge	The same initialized contents and read timing
Teaching aid	ROM INITIALIZATION AND LOOKUP TABLES - ADDRESS -> WRITE -> DATA_IN -> DATA_OUT -> VALID annotated concept and waveform view
Lab target	implement, predict, and verify rom initialization and lookup tables
Controls / actions	ten progressive activities using ADDRESS, WRITE, DATA_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for ROM initialization and lookup tables

Signals: ADDRESS, WRITE, DATA_IN, DATA_OUT, VALID	Interactive inputs: ADDRESS, WRITE, DATA_IN
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data transcript, boundary cases, and pass LED

Lesson 130 - 11.7 - True dual-port RAM behavior

Theme and objective	True dual-port RAM supports two independent controlled ports. Same-address collisions require a documented device-supported policy.
Complete example	`Port A writes address 5 while port B reads address 9; a collision test then exercises address 5.`
Learner action	What must the testbench check explicitly?
Expected knowledge	Same-address read/write collision behavior
Teaching aid	TRUE DUAL-PORT RAM BEHAVIOR - ADDRESS -> WRITE -> DATA_IN -> DATA_OUT -> VALID annotated concept and waveform view
Lab target	implement, predict, and verify true dual-port ram behavior
Controls / actions	ten progressive activities using ADDRESS, WRITE, DATA_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for True dual-port RAM behavior

Signals: ADDRESS, WRITE, DATA_IN, DATA_OUT, VALID	Interactive inputs: ADDRESS, WRITE, DATA_IN
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data transcript, boundary cases, and pass LED

Lesson 131 - 11.8 - FIFO depth, flags, and overflow

Theme and objective	FIFO sizing accounts for burst length and rate difference. Full, empty, almost-full, and level flags control safe transfers.
Complete example	`A producer stops before full; a consumer reads only when not empty.`
Learner action	What happens if a write is accepted while full?
Expected knowledge	Data may be lost unless the interface prevents it
Teaching aid	FIFO DEPTH, FLAGS, AND OVERFLOW - WRITE -> READ -> LEVEL -> FULL -> EMPTY annotated concept and waveform view
Lab target	implement, predict, and verify fifo depth, flags, and overflow
Controls / actions	ten progressive activities using WRITE, READ
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for FIFO depth, flags, and overflow

Signals: CLK, WRITE, READ, LEVEL, FULL, EMPTY	Interactive inputs: WRITE, READ
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data transcript, boundary cases, and pass LED

Lesson 132 - 11.9 - Fixed-point rounding and saturation

Theme and objective	Fixed-point arithmetic tracks binary points, growth, rounding, truncation, saturation, and overflow at every operation.
Complete example	`A wide accumulator is rounded before returning to an 8-bit saturated output.`
Learner action	Why saturate instead of wrap for some signals?
Expected knowledge	To clamp overflow to a defined maximum or minimum
Teaching aid	FIXED-POINT ROUNDING AND SATURATION - A -> B -> RESULT -> VALID -> OVERFLOW annotated concept and waveform view
Lab target	implement, predict, and verify fixed-point rounding and saturation
Controls / actions	ten progressive activities using A, B
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Fixed-point rounding and saturation

Signals: A, B, RESULT, VALID, OVERFLOW	Interactive inputs: A, B
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 133 - 11.10 - Memory and DSP accelerator capstone

Theme and objective	An accelerator streams samples from memory through pipelined DSP, stores results, and verifies numeric error, bandwidth, and overflow.
Complete example	`A small FIR engine reads coefficients from ROM and samples from RAM, then compares output with a reference model.`
Learner action	What evidence validates numerical behavior?
Expected knowledge	Reference comparison including boundary and overflow cases
Teaching aid	MEMORY AND DSP ACCELERATOR CAPSTONE - ADDRESS -> WRITE -> DATA_IN -> DATA_OUT -> VALID annotated concept and waveform view
Lab target	implement, predict, and verify memory and dsp accelerator capstone
Controls / actions	ten progressive activities using ADDRESS, WRITE, DATA_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Memory and DSP accelerator capstone

Signals: ADDRESS, WRITE, DATA_IN, DATA_OUT, VALID	Interactive inputs: ADDRESS, WRITE, DATA_IN
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data transcript, boundary cases, and pass LED

12 - Timing and Constraints

Constrain clocks and interfaces, then interpret timing reports correctly.

Lesson 134 - 12.1 - Primary clock constraints

Theme and objective	A clock constraint defines the period and waveform used by static timing analysis.
Complete example	`create_clock -period 10 [get_ports clk]`
Learner action	What frequency corresponds to 10 ns?
Expected knowledge	100 MHz
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Primary clock constraints
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 135 - 12.2 - Setup timing

Theme and objective	Setup analysis checks that data arrives sufficiently before the destination sampling edge.
Complete example	`slack = required time - arrival time`
Learner action	What does negative setup slack indicate?
Expected knowledge	Data arrives too late
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Setup timing
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 136 - 12.3 - Hold timing

Theme and objective	Hold analysis checks that data remains stable long enough after the same sampling edge.
Complete example	`Minimum-delay paths dominate hold checks`
Learner action	What commonly causes hold risk?
Expected knowledge	A path that is too fast
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Hold timing
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 137 - 12.4 - Input and output delays

Theme and objective	I/O delays describe timing outside the FPGA relative to the interface clock.
Complete example	`set_input_delay accounts for source device and board delay`
Learner action	Why constrain I/O?
Expected knowledge	To include external timing in analysis
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Input and output delays
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 138 - 12.5 - Timing exceptions

Theme and objective	False and multicycle paths are used only when the architecture proves the default timing relationship does not apply.
Complete example	`A two-cycle path gets a justified multicycle constraint`
Learner action	What is unsafe?
Expected knowledge	Adding exceptions only to hide violations
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Timing exceptions
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 139 - 12.6 - Generated clocks and clock relationships

Theme and objective	Derived clocks require constraints describing their source, divide/multiply ratio, phase, and intended relationships.
Complete example	`A divide-by-two supported clock output is constrained as generated from the primary source.`
Learner action	Why define the source clock relationship?
Expected knowledge	So timing analysis checks the correct launch and capture edges
Teaching aid	GENERATED CLOCKS AND CLOCK RELATIONSHIPS - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify generated clocks and clock relationships
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Generated clocks and clock relationships

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 140 - 12.7 - Clock groups and asynchronous domains

Theme and objective	Unrelated clocks are declared asynchronous only when crossings use approved CDC structures and are verified separately.
Complete example	`set_clock_groups separates two independent oscillator domains while an async FIFO protects data.`
Learner action	What is unsafe about declaring clocks asynchronous without CDC logic?
Expected knowledge	It hides real transfers from timing without making them safe
Teaching aid	CLOCK GROUPS AND ASYNCHRONOUS DOMAINS - ASYNC_IN -> SYNC1 -> SYNC2 -> EVENT annotated concept and waveform view
Lab target	implement, predict, and verify clock groups and asynchronous domains
Controls / actions	ten progressive activities using ASYNC_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Clock groups and asynchronous domains

Signals: CLK, ASYNC_IN, SYNC1, SYNC2, EVENT	Interactive inputs: ASYNC_IN
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 141 - 12.8 - Board-level input and output timing

Theme and objective	Input/output delays account for external device timing, board flight time, clock phase, and FPGA requirements.
Complete example	`A source-synchronous input constraint includes the transmitter clock-to-output and board margin.`
Learner action	What does set_input_delay model?
Expected knowledge	Timing outside the FPGA before the input pin
Teaching aid	BOARD-LEVEL INPUT AND OUTPUT TIMING - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify board-level input and output timing
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Board-level input and output timing

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 142 - 12.9 - CDC constraints and synchronizer review

Theme and objective	CDC review identifies every crossing, its protocol, synchronizer attributes, physical placement needs, and any justified timing exception.
Complete example	`A single-bit status uses two flops; a data bus uses a handshake or async FIFO.`
Learner action	Why not synchronize every bus bit independently?
Expected knowledge	Bits can be sampled from different source values
Teaching aid	CDC CONSTRAINTS AND SYNCHRONIZER REVIEW - ASYNC_IN -> SYNC1 -> SYNC2 -> EVENT annotated concept and waveform view
Lab target	implement, predict, and verify cdc constraints and synchronizer review
Controls / actions	ten progressive activities using ASYNC_IN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for CDC constraints and synchronizer review

Signals: CLK, ASYNC_IN, SYNC1, SYNC2, EVENT	Interactive inputs: ASYNC_IN
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 143 - 12.10 - Timing closure capstone

Theme and objective	Timing closure validates constraints, isolates true critical paths, improves architecture or implementation, and preserves functional correctness.
Complete example	`Pipeline a long datapath, rerun implementation, and compare setup/hold reports and latency tests.`
Learner action	What is the wrong way to close timing?
Expected knowledge	Add false paths only to hide violations
Teaching aid	TIMING CLOSURE CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify timing closure capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Timing closure capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

13 - Digital Interfaces

Implement and verify common board and peripheral protocols.

Lesson 144 - 13.1 - UART transmitter and receiver

Theme and objective	UART frames asynchronous serial data with start, data, optional parity, and stop bits.
Complete example	`start=0, eight data bits, stop=1`
Learner action	How does a receiver locate each bit?
Expected knowledge	It samples using the configured baud timing
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe UART transmitter and receiver
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: TX DATA, SERIAL TX, FRAME OK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	USB-UART terminal transcript and LED status

Lesson 145 - 13.2 - SPI controller

Theme and objective	SPI transfers synchronous serial data using SCLK, chip select, MOSI, and MISO with defined phase and polarity.
Complete example	`CPOL and CPHA select sampling edges`
Learner action	What activates one peripheral?
Expected knowledge	Its chip-select signal
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe SPI controller
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SCLK, MOSI, MISO	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	mikroBUS or loopback capture plus pass/fail LED

Lesson 146 - 13.3 - I2C open-drain bus

Theme and objective	I2C devices pull SDA and SCL low and rely on pull-ups for high, allowing arbitration and acknowledgement.
Complete example	`START is SDA falling while SCL is high`
Learner action	Why must outputs release high?
Expected knowledge	The shared bus uses open-drain signaling
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe I2C open-drain bus
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: SCL, SDA, ACK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	mikroBUS or loopback capture plus pass/fail LED

Lesson 147 - 13.4 - PWM generation

Theme and objective	PWM controls average output using a counter and a programmable duty comparison.
Complete example	`pwm = counter < duty;`
Learner action	What increases average high time?
Expected knowledge	A larger duty value
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe PWM generation
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result
Signals: CLK, COUNTER, DUTY, PWM	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants
PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 148 - 13.5 - AXI-Lite register bank

Theme and objective	A memory-mapped register bank accepts addressed reads and writes using independent handshake channels.
Complete example	`Software writes a control register; RTL drives hardware`
Learner action	What maps software to hardware state?
Expected knowledge	Addressed control and status registers
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe AXI-Lite register bank
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	SoftConsole or Linux console transcript plus fabric-controlled LED

Lesson 149 - 13.6 - Debounced GPIO and edge events

Theme and objective	Mechanical inputs require synchronization and debounce before edge detection. Outputs require documented polarity and safe reset values.
Complete example	`A button must remain stable for N cycles before one pressed event is generated.`
Learner action	What does debounce prevent?
Expected knowledge	Multiple events from contact bounce
Teaching aid	DEBOUNCED GPIO AND EDGE EVENTS - INPUT_PIN -> INTERNAL -> OUTPUT_PIN -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify debounced gpio and edge events
Controls / actions	ten progressive activities using INPUT_PIN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Debounced GPIO and edge events

Signals: INPUT_PIN, INTERNAL, OUTPUT_PIN, OBSERVED	Interactive inputs: INPUT_PIN
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 150 - 13.7 - SPI mode and transaction engine

Theme and objective	An SPI engine defines CPOL, CPHA, word length, bit order, chip-select timing, and completion/error behavior.
Complete example	`Mode 0 samples MISO on rising SCLK and shifts MOSI on the opposite edge.`
Learner action	What must match the peripheral?
Expected knowledge	Clock mode, bit order, and transaction timing
Teaching aid	SPI MODE AND TRANSACTION ENGINE - SCLK -> CS_N -> MOSI -> MISO -> DONE annotated concept and waveform view
Lab target	implement, predict, and verify spi mode and transaction engine
Controls / actions	ten progressive activities using CS_N, MOSI
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for SPI mode and transaction engine

Signals: SCLK, CS_N, MOSI, MISO, DONE	Interactive inputs: CS_N, MOSI
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	protocol capture, transaction log, and pass/fail LED

Lesson 151 - 13.8 - I2C arbitration and acknowledgement

Theme and objective	I2C uses open-drain SDA/SCL, START/STOP conditions, address phases, ACK/NACK, clock stretching, and arbitration.
Complete example	`The master releases SDA for ACK and samples whether the receiver pulls it low.`
Learner action	What does NACK indicate?
Expected knowledge	The receiver did not acknowledge that byte
Teaching aid	I2C ARBITRATION AND ACKNOWLEDGEMENT - SCL -> SDA -> ACK -> BUSY -> ERROR annotated concept and waveform view
Lab target	implement, predict, and verify i2c arbitration and acknowledgement
Controls / actions	ten progressive activities using SCL, SDA
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for I2C arbitration and acknowledgement

Signals: SCL, SDA, ACK, BUSY, ERROR	Interactive inputs: SCL, SDA
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	protocol capture, transaction log, and pass/fail LED

Lesson 152 - 13.9 - Robust UART receive path

Theme and objective	A UART receiver synchronizes RX, detects start, samples near bit centers, shifts data, and validates stop/parity with error flags.
Complete example	`A 16x tick generator samples the start bit and then each data bit near its center.`
Learner action	What should a bad stop bit produce?
Expected knowledge	A framing error
Teaching aid	ROBUST UART RECEIVE PATH - RX -> TX -> VALID -> ERROR annotated concept and waveform view
Lab target	implement, predict, and verify robust uart receive path
Controls / actions	ten progressive activities using RX
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Robust UART receive path

Signals: RX, TX, VALID, ERROR	Interactive inputs: RX
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	UART transcript, error status, and pass LED

Lesson 153 - 13.10 - Multi-interface peripheral capstone

Theme and objective	A complete peripheral subsystem combines addressed control registers, protocol engines, buffering, interrupts, status, reset, and board loopback tests.
Complete example	`Software configures SPI, a FIFO buffers bytes, and UART reports transaction status.`
Learner action	What keeps software and RTL consistent?
Expected knowledge	A documented register map and handshake contract
Teaching aid	MULTI-INTERFACE PERIPHERAL CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify multi-interface peripheral capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Multi-interface peripheral capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

14 - PolarFire Architecture

Map RTL decisions onto Microchip PolarFire resources.

Lesson 154 - 14.1 - Logic elements and routing

Theme and objective	PolarFire fabric combines logic, registers, and programmable routing to implement RTL networks.
Complete example	`Boolean logic maps into fabric logic elements`
Learner action	Where does combinational RTL map?
Expected knowledge	Fabric logic and routing
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Logic elements and routing
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 155 - 14.2 - Clock conditioning circuits

Theme and objective	Dedicated clock resources distribute low-skew clocks and provide supported frequency conditioning.
Complete example	`Reference clock -> CCC/PLL -> global clock`
Learner action	Why avoid fabric-generated clocks?
Expected knowledge	They can have uncontrolled skew and timing
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Clock conditioning circuits
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, D, Q	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 156 - 14.3 - LSRAM and uSRAM

Theme and objective	PolarFire provides embedded memory resources with different capacities and configurations.
Complete example	`Select memory style from required depth, width, and ports`
Learner action	What should guide memory selection?
Expected knowledge	Capacity, ports, and timing needs
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe LSRAM and uSRAM
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: ADDRESS, DATA, VALID	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	written/read data reported over UART with a pass/fail LED

Lesson 157 - 14.4 - Transceivers and high-speed I/O

Theme and objective	Device variants provide hardened high-speed resources that require reference clocks and protocol-aware constraints.
Complete example	`SERDES path uses dedicated transceiver resources`
Learner action	What is required beyond ordinary GPIO?
Expected knowledge	A supported transceiver configuration
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Transceivers and high-speed I/O
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	PRBS/link status, error count, and SmartDebug capture

Lesson 158 - 14.5 - Security and nonvolatile configuration

Theme and objective	PolarFire combines nonvolatile fabric configuration with device security features and controlled programming flows.
Complete example	`Programming policy protects design assets`
Learner action	What should a project define?
Expected knowledge	A deliberate security and provisioning policy
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Security and nonvolatile configuration
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 159 - 14.6 - PolarFire clock resource planning

Theme and objective	Clock sources, CCC/PLL resources, global networks, domain frequencies, reset release, and clock consumers are planned before implementation.
Complete example	`One board oscillator feeds a CCC that produces separately constrained fabric clocks.`
Learner action	What should never be assumed from a clock net name?
Expected knowledge	Its actual frequency and source
Teaching aid	POLARFIRE CLOCK RESOURCE PLANNING - D -> ENABLE -> Q annotated concept and waveform view
Lab target	implement, predict, and verify polarfire clock resource planning
Controls / actions	ten progressive activities using D, ENABLE
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for PolarFire clock resource planning

Signals: CLK, D, ENABLE, Q	Interactive inputs: D, ENABLE
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 160 - 14.7 - PolarFire I/O bank planning

Theme and objective	I/O assignment respects package availability, bank voltage, electrical standard, differential pairing, board nets, and reserved functions.
Complete example	`Group compatible LVCMOS ports into a bank powered for their required standard.`
Learner action	What can make a package pin unusable for a chosen port?
Expected knowledge	Bank, voltage, pairing, or reserved-function constraints
Teaching aid	POLARFIRE I/O BANK PLANNING - INPUT_PIN -> INTERNAL -> OUTPUT_PIN -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify polarfire i/o bank planning
Controls / actions	ten progressive activities using INPUT_PIN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for PolarFire I/O bank planning

Signals: INPUT_PIN, INTERNAL, OUTPUT_PIN, OBSERVED	Interactive inputs: INPUT_PIN
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 161 - 14.8 - Nonvolatile fabric and device security

Theme and objective	PolarFire nonvolatile configuration and security features require deliberate lifecycle, programming, debug, and asset-protection decisions.
Complete example	`A training project records image identity and uses no production secrets.`
Learner action	What belongs in a security plan?
Expected knowledge	Provisioning, debug, update, and recovery policy
Teaching aid	NONVOLATILE FABRIC AND DEVICE SECURITY - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify nonvolatile fabric and device security
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Nonvolatile fabric and device security

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 162 - 14.9 - PolarFire resource budget

Theme and objective	A resource budget allocates logic, registers, memories, DSP, clocks, I/O, and timing margin per subsystem before integration.
Complete example	`Reserve memory and DSP for the datapath plus headroom for control and debug.`
Learner action	Why keep implementation headroom?
Expected knowledge	Integration, routing, debug, and revisions need margin
Teaching aid	POLARFIRE RESOURCE BUDGET - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify polarfire resource budget
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for PolarFire resource budget

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 163 - 14.10 - Architecture mapping capstone

Theme and objective	A PolarFire architecture review maps every requirement to fabric, memory, DSP, clocks, I/O, security, and observable board evidence.
Complete example	`Review a streaming controller block diagram against resource, clock, interface, and verification budgets.`
Learner action	What closes the architecture review?
Expected knowledge	Traceable requirements, budgets, interfaces, risks, and evidence
Teaching aid	ARCHITECTURE MAPPING CAPSTONE - INPUT_PIN -> INTERNAL -> OUTPUT_PIN -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify architecture mapping capstone
Controls / actions	ten progressive activities using INPUT_PIN
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Architecture mapping capstone

Signals: INPUT_PIN, INTERNAL, OUTPUT_PIN, OBSERVED	Interactive inputs: INPUT_PIN
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

15 - Libero SoC Workflow

Take a reviewed RTL design through Microchip implementation tools.

Lesson 164 - 15.1 - Project and device setup

Theme and objective	The Libero project must target the exact family, device, package, and speed grade used by the board.
Complete example	`Board documentation identifies the fitted FPGA`
Learner action	Why select the exact part?
Expected knowledge	Resources, pins, and timing models depend on it
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Project and device setup
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 165 - 15.2 - SmartDesign integration

Theme and objective	SmartDesign connects RTL, generated IP, clocks, resets, and interfaces in a reviewable system diagram.
Complete example	`Instantiate a CCC and connect its locked output to reset logic`
Learner action	What does SmartDesign capture?
Expected knowledge	System-level component connectivity
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe SmartDesign integration
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 166 - 15.3 - I/O and timing constraints

Theme and objective	PDC and SDC constraints connect logical ports to board pins and define required timing.
Complete example	`Assign LED port, I/O standard, and primary clock`
Learner action	What must be checked against the board?
Expected knowledge	Pin mapping and electrical standard
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe I/O and timing constraints
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: SOURCE, DESTINATION, SLACK PASS	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing report and measured GPIO/LED behavior

Lesson 167 - 15.4 - Synthesis and place-and-route reports

Theme and objective	Reports reveal inferred resources, warnings, utilization, clocking, and timing results.
Complete example	`Review warnings before accepting a green status icon`
Learner action	What requires investigation?
Expected knowledge	Unexpected latches, clocks, or unconstrained paths
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Synthesis and place-and-route reports
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 168 - 15.5 - Programming and hardware debug

Theme and objective	Program the generated image, apply a written test plan, and compare measured hardware with simulation.
Complete example	`Use LEDs, UART, or an embedded logic analyzer for evidence`
Learner action	What closes the verification loop?
Expected knowledge	Repeatable board results matching expected behavior
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Programming and hardware debug
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 169 - 15.6 - SmartDesign IP configuration

Theme and objective	Generated IP is configured with explicit parameters, versions, clocks, resets, interfaces, and generated constraints, then reviewed as part of the design.
Complete example	`Configure a CCC, record its input/output frequencies, and connect lock to reset sequencing.`
Learner action	What must be version-controlled for generated IP?
Expected knowledge	Configuration, versions, generated files, and integration settings
Teaching aid	SMARTDESIGN IP CONFIGURATION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify smartdesign ip configuration
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for SmartDesign IP configuration

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 170 - 15.7 - Import and audit PDC and SDC

Theme and objective	Constraint files are imported in the intended order and audited for exact ports, clocks, I/O standards, exceptions, and unresolved placeholders.
Complete example	`The build fails if PIN_FROM_CURRENT_BOARD_GUIDE remains in a PDC.`
Learner action	When may a placeholder pin be accepted?
Expected knowledge	Never in a programming build
Teaching aid	IMPORT AND AUDIT PDC AND SDC - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify import and audit pdc and sdc
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Import and audit PDC and SDC

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 171 - 15.8 - Resolve synthesis warnings

Theme and objective	Warnings about latches, width truncation, multiple drivers, unused logic, inferred clocks, and undriven nets are resolved or documented.
Complete example	`A width warning leads to explicit extension or a documented intentional truncation.`
Learner action	What is a warning disposition?
Expected knowledge	A recorded cause, decision, and impact
Teaching aid	RESOLVE SYNTHESIS WARNINGS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify resolve synthesis warnings
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Resolve synthesis warnings

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 172 - 15.9 - SmartDebug and on-board observation

Theme and objective	Hardware debug uses observable signals, triggers, status counters, UART logs, and supported tools without changing the intended function invisibly.
Complete example	`Trigger on an error flag and capture state, control, and data around the event.`
Learner action	What makes a useful trigger?
Expected knowledge	It isolates the event tied to a requirement or failure
Teaching aid	SMARTDEBUG AND ON-BOARD OBSERVATION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify smartdebug and on-board observation
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for SmartDebug and on-board observation

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 173 - 15.10 - Reproducible Libero build capstone

Theme and objective	A reproducible build records source revision, Libero/device versions, IP configuration, constraints, scripts, warnings, reports, and programming digest.
Complete example	`A clean workspace rebuild produces equivalent reports and the recorded image digest.`
Learner action	What should another engineer be able to do?
Expected knowledge	Rebuild and verify the same design from the archive
Teaching aid	REPRODUCIBLE LIBERO BUILD CAPSTONE - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify reproducible libero build capstone
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Reproducible Libero build capstone

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

16 - Capstone FPGA Systems

Combine design, verification, timing, and board evidence in complete projects.

Lesson 174 - 16.1 - Traffic-light controller

Theme and objective	A timed FSM coordinates mutually exclusive outputs, reset behavior, and safe transitions.
Complete example	`RED -> RED_AMBER -> GREEN -> AMBER`
Learner action	What must verification prove?
Expected knowledge	No unsafe light combination occurs
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Traffic-light controller
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, INPUT, STATE, OUTPUT	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 175 - 16.2 - UART command console

Theme and objective	A UART receiver, parser, register bank, and transmitter form a controllable debug interface.
Complete example	`Command writes PWM duty; response returns status`
Learner action	Which block stores settings?
Expected knowledge	The command register bank
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe UART command console
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: TX DATA, SERIAL TX, FRAME OK	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	USB-UART terminal transcript and LED status

Lesson 176 - 16.3 - Sensor acquisition pipeline

Theme and objective	A sampled interface feeds filtering, thresholding, buffering, and timestamp logic with valid flow control.
Complete example	`SPI sample -> filter -> threshold -> FIFO`
Learner action	Why propagate valid?
Expected knowledge	To identify which cycles contain meaningful data
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe Sensor acquisition pipeline
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: CLK, STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: clocked	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 177 - 16.4 - FIR filter accelerator

Theme and objective	A pipelined multiply-accumulate architecture maps taps into DSP and memory resources.
Complete example	`Each sample advances through coefficient taps`
Learner action	What sets numerical accuracy?
Expected knowledge	Coefficient and accumulator widths
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe FIR filter accelerator
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 178 - 16.5 - PolarFire board final project

Theme and objective	The final project includes requirements, RTL, self-checking simulation, constraints, timing closure, programming, and measured evidence.
Complete example	`Deliver source, tests, reports, bitstream record, and board checklist`
Learner action	What demonstrates completion?
Expected knowledge	Requirements traced to simulation, timing, and board results
Teaching aid	Interactive concept diagram and live signal graph
Lab target	Implement and observe PolarFire board final project
Controls / actions	Apply controlled stimulus and compare the output
Required lab evidence	Verified waveform and explained result

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: Guided lesson-specific stimulus
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-switch/push-button stimulus and the expected LED or GPIO result

Lesson 179 - 16.6 - Capstone requirements and acceptance tests

Theme and objective	Capstone requirements are measurable and each has an acceptance test, expected result, evidence format, and owner.
Complete example	`Requirement R7: accept one sample per cycle for 1024 cycles without loss; test counts accepted and produced samples.`
Learner action	What makes an acceptance criterion useful?
Expected knowledge	It is objective, measurable, and reproducible
Teaching aid	CAPSTONE REQUIREMENTS AND ACCEPTANCE TESTS - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify capstone requirements and acceptance tests
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Capstone requirements and acceptance tests

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 180 - 16.7 - Capstone architecture partition

Theme and objective	The system is partitioned into datapath, control, memories, interfaces, clock/reset domains, software boundary, debug, and verification hooks.
Complete example	`A block diagram labels every interface width, direction, clock domain, and backpressure rule.`
Learner action	What must be defined at every block boundary?
Expected knowledge	Interface, timing domain, ownership, and protocol
Teaching aid	CAPSTONE ARCHITECTURE PARTITION - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify capstone architecture partition
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Capstone architecture partition

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 181 - 16.8 - Capstone verification plan

Theme and objective	The plan maps requirements to directed, randomized, assertion, coverage, fault, reset, performance, and board tests.
Complete example	`Each requirement links to at least one automatic simulation check and one relevant acceptance artifact.`
Learner action	How is a verification gap found?
Expected knowledge	A requirement has no adequate planned check or coverage
Teaching aid	CAPSTONE VERIFICATION PLAN - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify capstone verification plan
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Capstone verification plan

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

Lesson 182 - 16.9 - Capstone timing and resource review

Theme and objective	Before hardware release, reviewers examine constraints, clocks, CDC, setup/hold, utilization, critical paths, power estimate, and headroom.
Complete example	`A documented review rejects unexplained unconstrained paths even when the functional simulation passes.`
Learner action	What does functional simulation not prove?
Expected knowledge	Physical timing closure and safe CDC implementation
Teaching aid	CAPSTONE TIMING AND RESOURCE REVIEW - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify capstone timing and resource review
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Capstone timing and resource review

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing clock/timing report and measured GPIO or LED behavior

Lesson 183 - 16.10 - Integrated FPGA delivery review

Theme and objective	The final delivery connects requirements, architecture, RTL, tests, coverage, constraints, reports, programming image, measurements, limitations, and maintenance instructions.
Complete example	`Demonstrate reset, nominal load, boundary load, backpressure, injected fault, recovery, throughput, and reproducible reprogramming.`
Learner action	What distinguishes a professional delivery?
Expected knowledge	Traceable claims supported by repeatable simulation and board evidence
Teaching aid	INTEGRATED FPGA DELIVERY REVIEW - STIMULUS -> EXPECTED -> OBSERVED annotated concept and waveform view
Lab target	implement, predict, and verify integrated fpga delivery review
Controls / actions	ten progressive activities using STIMULUS
Required lab evidence	prediction, annotated waveform, automated check, and discrepancy explanation for Integrated FPGA delivery review

Signals: STIMULUS, EXPECTED, OBSERVED	Interactive inputs: STIMULUS
In-app controls: combinational / conceptual	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch/button stimulus, expected LED/GPIO result, and explained observation

17 - Advanced SystemVerilog RTL

Build strongly typed, reusable, reviewable hardware modules.

Lesson 184 - 17.1 - Typed ports and logic signals

Theme and objective	SystemVerilog logic ports make direction and width explicit. One signal must still have one intended driver.
Complete example	`module mask(input logic [7:0] sw, output logic [7:0] led); assign led = sw; endmodule`
Learner action	Which declaration carries eight input bits?
Expected knowledge	input logic [7:0] sw
Teaching aid	SW[7:0] -- typed input port --> LED[7:0] width=8, direction=input
Lab target	an eight-bit typed pass-through
Controls / actions	SW[7:0] stimulus and declared widths
Required lab evidence	LED[7:0] equality and clean compile log

Signals: SW0, SW1, LED0, LED1	Interactive inputs: SW0, SW1
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	all eight DIP switches reproduced on LED1-LED8

Lesson 185 - 17.2 - Signed arithmetic and extension

Theme and objective	Signed operands require deliberate extension so sign, carry, and overflow are not confused.
Complete example	`logic signed [7:0] a,b; logic signed [8:0] wide_sum; assign wide_sum = a + b;`
Learner action	Why is wide_sum nine bits?
Expected knowledge	To retain the extended arithmetic result
Teaching aid	A[7:0] -+ +- signed 9-bit ADD -> SUM[8:0], OVF B[7:0] -+
Lab target	a signed add/subtract datapath
Controls / actions	two signed switch operands and operation select
Required lab evidence	UART result, sign, carry, and overflow record

Signals: CLK, A7, A0, B7, B0, SUM, OVF	Interactive inputs: A7, A0, B7, B0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch-selected signed cases printed over USB-UART

Lesson 186 - 17.3 - Enumerated states

Theme and objective	An enum gives each legal FSM state a meaningful name and a controlled encoding width.
Complete example	`typedef enum logic [1:0] {IDLE, LOAD, RUN, DONE} state_t;`
Learner action	What benefit does state_t provide?
Expected knowledge	Named legal states with an explicit encoding width
Teaching aid	IDLE -start-> LOAD -ready-> RUN -done-> DONE ^ | +---------- reset ----------+
Lab target	a four-state sequencer
Controls / actions	START, READY, and DONE switch events
Required lab evidence	state code and transition trace

Signals: CLK, START, READY, DONE, S0, S1	Interactive inputs: START, READY, DONE, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	buttons advance named states displayed on two LEDs

Lesson 187 - 17.4 - Packed structs for transactions

Theme and objective	A packed struct groups related fields into one synthesizable bus while preserving field names.
Complete example	`typedef struct packed {logic valid; logic [3:0] tag; logic [7:0] data;} packet_t;`
Learner action	How many bits does packet_t contain?
Expected knowledge	13 bits
Teaching aid	[VALID|TAG 4|DATA 8] = one 13-bit packed transaction
Lab target	a tagged transaction register
Controls / actions	VALID, TAG, DATA, and capture enable
Required lab evidence	captured packet fields reported over UART

Signals: CLK, VALID, TAG0, DATA0, QVALID, QDATA	Interactive inputs: VALID, TAG0, DATA0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DIP-selected packet captured by button and decoded over UART

Lesson 188 - 17.5 - Interfaces and modports

Theme and objective	An interface bundles a protocol; modports restrict which side drives each signal.
Complete example	`modport source(output valid,data, input ready); modport sink(input valid,data, output ready);`
Learner action	Which side drives ready in this example?
Expected knowledge	The sink
Teaching aid	SOURCE [valid,data] -----> SINK SOURCE <---------- [ready] SINK
Lab target	a typed valid-ready channel
Controls / actions	VALID, READY, and DATA controls
Required lab evidence	transfer count with no ownership violation

Signals: CLK, VALID, READY, DATA, XFER	Interactive inputs: VALID, READY, DATA
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch-driven source and button-driven sink increment a transfer LED counter

Lesson 189 - 17.6 - Packages and pure functions

Theme and objective	Packages centralize shared types and constants. A synthesizable function expresses reusable combinational calculation.
Complete example	`function automatic logic parity8(input logic [7:0] d); return ^d; endfunction`
Learner action	What hardware does ^d describe?
Expected knowledge	Reduction XOR parity
Teaching aid	DATA[7:0] -> parity8() -> PARITY shared package definition
Lab target	a reusable parity function
Controls / actions	all eight DIP switches
Required lab evidence	parity LED and exhaustive simulation pass count

Signals: D0, D1, D2, D3, PARITY	Interactive inputs: D0, D1, D2, D3
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	LED parity changes correctly for multiple eight-switch patterns

Lesson 190 - 17.7 - Generate loops and arrays

Theme and objective	A generate loop elaborates repeated hardware instances; it does not execute repeatedly at run time.
Complete example	`for (genvar i=0; i<8; i++) assign led[i] = sw[i] & enable;`
Learner action	How many AND channels are elaborated?
Expected knowledge	Eight
Teaching aid	SW[i] -+- AND -> LED[i] repeated for i=0..7 ENABLE -+
Lab target	an eight-channel generated bank
Controls / actions	ENABLE plus SW[7:0]
Required lab evidence	eight independent LED channel results

Signals: EN, SW0, SW7, LED0, LED7	Interactive inputs: EN, SW0, SW7
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	ENABLE gates all eight DIP-to-LED channels simultaneously

Lesson 191 - 17.8 - Parameter guards and width contracts

Theme and objective	Reusable modules must reject illegal parameter values and calculate internal widths safely.
Complete example	`localparam AW = $clog2(DEPTH); initial assert (DEPTH > 1);`
Learner action	What does $clog2(DEPTH) determine?
Expected knowledge	The address width required for DEPTH entries
Teaching aid	DEPTH -> $clog2 -> ADDRESS WIDTH | +- assertion rejects illegal configuration
Lab target	a parameterized depth counter
Controls / actions	DEPTH variants and boundary count values
Required lab evidence	compile-time guard and correct rollover

Signals: CLK, EN, MAX, COUNT, WRAP	Interactive inputs: EN, MAX
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	two synthesized width variants show correct LED rollover

Lesson 192 - 17.9 - Combinational completeness and latch prevention

Theme and objective	Every combinational output needs an assignment on every path. Defaults plus overrides make that coverage visible.
Complete example	`always_comb begin y = 0; if (enable) y = data; end`
Learner action	What happens when enable is zero?
Expected knowledge	y receives the explicit default zero
Teaching aid	DEFAULT Y=0 -> if ENABLE then Y=DATA Every path assigns Y
Lab target	a latch-free conditional datapath
Controls / actions	ENABLE and DATA boundary cases
Required lab evidence	zero latch warnings and immediate LED response

Signals: EN, DATA, Y, LATCH_WARN	Interactive inputs: EN, DATA
In-app controls: multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	LED responds combinationally with no synthesis latch report

Lesson 193 - 17.10 - Reusable RTL IP review

Theme and objective	Professional RTL IP combines a clear contract, typed ports, parameter rules, reset behavior, assertions, and reproducible tests.
Complete example	`Review checklist: interface, widths, reset, CDC, warnings, tests, constraints, hardware evidence.`
Learner action	Which artifact defines how another module may use the IP?
Expected knowledge	The documented interface contract
Teaching aid	CONTRACT -> RTL -> ASSERTIONS -> SYNTHESIS -> BOARD trace every requirement end-to-end
Lab target	a reviewed reusable GPIO processing IP
Controls / actions	parameter, reset, enable, and data cases
Required lab evidence	review checklist, regression log, timing report, and board capture

Signals: CLK, RST, EN, DATA, VALID, RESULT	Interactive inputs: EN, DATA, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	versioned Libero component drives LEDs and reports self-test over UART

18 - Clocking, Reset, and CDC

Engineer clocks, resets, and safe transfers between timing domains.

Lesson 194 - 18.1 - Board oscillator and global clock network

Theme and objective	A board oscillator enters a clock-capable pin and reaches sequential logic through dedicated low-skew clock resources.
Complete example	`board oscillator -> clock input -> global buffer -> registers`
Learner action	Why use the dedicated global network?
Expected knowledge	To distribute the clock with controlled skew
Teaching aid	OSC -> CLK IN -> GLOBAL CLOCK -+> FF bank A +> FF bank B
Lab target	a global-clock heartbeat counter
Controls / actions	clock constraint and counter division value
Required lab evidence	measured LED heartbeat and reported clock period

Signals: CLK, EN, CLK_OK, COUNT, LED	Interactive inputs: EN
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	scope or timed video of the divided heartbeat LED

Lesson 195 - 18.2 - CCC and PLL frequency generation

Theme and objective	PolarFire clock conditioning resources generate supported frequencies and expose lock status for controlled release of logic.
Complete example	`reference clock -> CCC/PLL -> generated clock; LOCK gates startup reset release`
Learner action	When may dependent logic leave reset?
Expected knowledge	After the generated clock is stable and lock is asserted
Teaching aid	REFCLK -> CCC/PLL -> CLK_OUT +------> LOCK -> reset release
Lab target	a conditioned-clock startup controller
Controls / actions	frequency selection and simulated LOCK delay
Required lab evidence	LOCK trace, clock measurement, and stable counter

Signals: CLK, SEL, LOCK, CLK_OK, LED	Interactive inputs: SEL, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	SmartDebug/oscilloscope clock measurement and LOCK status LED

Lesson 196 - 18.3 - Synchronous reset sequencing

Theme and objective	A synchronous reset changes state only on the active clock edge and must meet timing like other synchronous controls.
Complete example	`always_ff @(posedge clk) if (rst) q <= 0; else q <= d;`
Learner action	When does q clear?
Expected knowledge	On a rising edge while rst is asserted
Teaching aid	RST --------+ CLK _/-_/-_ +- sample reset at edge -> Q=0 D -----------+
Lab target	a synchronously reset register bank
Controls / actions	RST, D, and clock-edge sequences
Required lab evidence	Q clears only at documented edges

Signals: CLK, D, RST, Q, VALID	Interactive inputs: D, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	push-button reset captured at clock edges and shown on LEDs

Lesson 197 - 18.4 - Asynchronous assert, synchronous release

Theme and objective	A common reset strategy asserts immediately but passes deassertion through synchronizing flip-flops in each clock domain.
Complete example	`async reset clears sync_ff; two clock edges shift a safe release high`
Learner action	Why synchronize deassertion?
Expected knowledge	To prevent different registers leaving reset on unsafe edges
Teaching aid	RESET_N -> async clear [FF1->FF2] -> DOMAIN_RESET_N clocked release
Lab target	a two-stage reset release synchronizer
Controls / actions	asynchronous button timing around clock edges
Required lab evidence	immediate assertion and two-edge release trace

Signals: CLK, RESET_N, RST_SYNC, READY	Interactive inputs: RESET_N
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	reset button forces immediate LED clear and deterministic delayed restart

Lesson 198 - 18.5 - Two-flop single-bit synchronizer

Theme and objective	A single asynchronous level is sampled by a destination-domain flip-flop and then a second flip-flop to reduce metastability propagation risk.
Complete example	`async_in -> sync_ff1 -> sync_ff2 -> destination logic`
Learner action	Which signal should destination logic consume?
Expected knowledge	sync_ff2
Teaching aid	ASYNC_IN -> FF1 -> FF2 -> SAFE_LEVEL destination clock domain
Lab target	a single-bit level synchronizer
Controls / actions	asynchronous switch transitions
Required lab evidence	source, first-stage, and safe-level traces

Signals: CLK, ASYNC, FF1, SAFE	Interactive inputs: ASYNC
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	asynchronous button changes a synchronized LED without combinational crossing

Lesson 199 - 18.6 - Pulse transfer with a toggle synchronizer

Theme and objective	A narrow source pulse can be encoded as a persistent toggle, synchronized, and edge-detected in the destination domain.
Complete example	`source pulse toggles bit -> 2FF sync -> XOR delayed copy creates destination pulse`
Learner action	Why encode the pulse as a toggle?
Expected knowledge	The state change persists long enough to be sampled
Teaching aid	SRC_PULSE -> TOGGLE -> [FF1->FF2] -> XOR -> DST_PULSE
Lab target	a reliable pulse-domain crossing
Controls / actions	source pulse spacing versus destination clock
Required lab evidence	one destination pulse for every accepted source event

Signals: CLK, PULSE, TOGGLE, SYNC, DST_PULSE	Interactive inputs: PULSE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button events in one divided clock domain increment an LED counter in another

Lesson 200 - 18.7 - Gray-code counter crossing

Theme and objective	Gray encoding changes one bit per adjacent count, reducing ambiguity when a multi-bit pointer is synchronized.
Complete example	`gray = binary ^ (binary >> 1); 0111 binary -> 0100 Gray`
Learner action	How many Gray pointer bits should change per increment?
Expected knowledge	One
Teaching aid	BINARY COUNTER -> XOR SHIFT -> GRAY -> bit synchronizers
Lab target	a Gray-coded event counter crossing
Controls / actions	increment enable and two independent clock rates
Required lab evidence	adjacent one-bit Gray transitions and reconstructed count

Signals: CLK, INC, G0, G1, G2, COUNT_OK	Interactive inputs: INC
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	LED Gray sequence advances one bit at a time under button control

Lesson 201 - 18.8 - Asynchronous FIFO architecture

Theme and objective	An asynchronous FIFO combines dual-port memory, local binary pointers, synchronized Gray pointers, and full/empty logic.
Complete example	`write clock/domain -> RAM <- read clock/domain; Gray pointers cross between them`
Learner action	Which data structure preserves multi-bit payload coherency?
Expected knowledge	The dual-port memory controlled by synchronized pointers
Teaching aid	WR_CLK: DATA->RAM, WR_PTR_GRAY -----> FULL/EMPTY RD_CLK: DATA<-RAM, <----- RD_PTR_GRAY
Lab target	a dual-clock asynchronous FIFO
Controls / actions	independent write/read enables and rates
Required lab evidence	ordered UART readback with correct full/empty flags

Signals: CLK, WR_EN, RD_EN, FULL, EMPTY, DATA_OK	Interactive inputs: WR_EN, RD_EN
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch values queued at one clock rate and printed in order at another

Lesson 202 - 18.9 - CDC constraints and structural review

Theme and objective	CDC safety needs both correct RTL structures and constraints that identify asynchronous clocks and synchronizer intent.
Complete example	`Declare unrelated clocks asynchronous; inspect that only approved synchronizers cross the boundary.`
Learner action	What is not sufficient by itself?
Expected knowledge	A false-path constraint without a safe CDC circuit
Teaching aid	CLOCK GROUPS + CDC STRUCTURE + MTBF REVIEW All three must agree
Lab target	a constrained two-clock crossing report
Controls / actions	clock relationship and crossing classification
Required lab evidence	zero unreviewed CDC paths and documented exceptions

Signals: CLK, SRC_EVENT, DST_EVENT, CDC_OK	Interactive inputs: SRC_EVENT
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Libero CDC/timing reports packaged with a functioning cross-domain LED demo

Lesson 203 - 18.10 - Multi-clock acquisition capstone

Theme and objective	A complete multi-clock system combines conditioned clocks, reset release, a safe control synchronizer, and an asynchronous data FIFO.
Complete example	`sensor clock -> sample FIFO -> processing clock -> result UART`
Learner action	Which crossing carries the sample bus safely?
Expected knowledge	The asynchronous FIFO
Teaching aid	SENSOR_CLK -> ACQUIRE -> ASYNC FIFO -> PROCESS -> UART resets released per domain
Lab target	a two-clock sensor acquisition pipeline
Controls / actions	sample enable, rate ratio, reset, and backpressure
Required lab evidence	ordered samples, clean CDC report, timing pass, and UART capture

Signals: CLK, SAMPLE, READY, FULL, VALID, RESULT	Interactive inputs: SAMPLE, READY, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit fabric streams switch samples across domains to USB-UART

19 - Verification and Formal Reasoning

Create self-checking, coverage-driven, assertion-based verification.

Lesson 204 - 19.1 - Verification plan from requirements

Theme and objective	A verification plan turns every design requirement into stimulus, checks, coverage, and completion evidence.
Complete example	`REQ-04 FIFO ordering -> directed sequence + scoreboard + ordering assertion + coverpoint`
Learner action	What makes a requirement verified?
Expected knowledge	A passing check with traceable coverage evidence
Teaching aid	REQUIREMENT -> TEST -> CHECK -> COVERAGE -> EVIDENCE
Lab target	a traceable verification plan
Controls / actions	requirement IDs and planned scenarios
Required lab evidence	requirements-to-results matrix

Signals: CLK, STIM, CHECK, COVER, PASS	Interactive inputs: STIM
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	board acceptance checklist linked to each simulated requirement

Lesson 205 - 19.2 - Constrained stimulus generation

Theme and objective	Constrained stimulus produces legal combinations across a useful range while preserving repeatable random seeds.
Complete example	`Randomize packet length 1..16 and opcode in the supported set; record seed 42017.`
Learner action	Why record the random seed?
Expected knowledge	To reproduce the exact failing sequence
Teaching aid	SEED -> CONSTRAINTS -> LEGAL TRANSACTIONS -> DUT
Lab target	a repeatable transaction generator
Controls / actions	seed, opcode set, length range, and invalid-case injection
Required lab evidence	stimulus log and reproducible failure ID

Signals: CLK, VALID, OP0, LEN0, ACCEPT	Interactive inputs: VALID, OP0, LEN0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	same seeded vectors replayed through switches/UART into the programmed DUT

Lesson 206 - 19.3 - Reference models and scoreboards

Theme and objective	A reference model independently predicts results; a scoreboard matches expected and actual transactions despite latency.
Complete example	`expected_queue.push(model(input)); compare when output_valid arrives;`
Learner action	Why queue expected results?
Expected knowledge	To align predictions with delayed DUT outputs
Teaching aid	INPUT -+-> DUT ---------> ACTUAL -+ +-> MODEL -> EXPECTED QUEUE -+- COMPARE
Lab target	a latency-aware scoreboard
Controls / actions	data, valid, ready, and injected pipeline delay
Required lab evidence	transaction-by-transaction match log

Signals: CLK, VALID, READY, EXPECTED, ACTUAL, MATCH	Interactive inputs: VALID, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	UART self-test reports expected/actual values and zero mismatches

Lesson 207 - 19.4 - Immediate and concurrent assertions

Theme and objective	Immediate assertions check a value now; concurrent assertions describe clocked relationships across time.
Complete example	`assert property (@(posedge clk) valid && !ready |=> valid);`
Learner action	What must remain asserted while backpressured?
Expected knowledge	valid
Teaching aid	valid && !ready at cycle N -> valid at cycle N+1
Lab target	a valid-ready protocol assertion set
Controls / actions	backpressure length and data stability
Required lab evidence	assertion pass/fail report with first failing cycle

Signals: CLK, VALID, READY, STABLE, ASSERT_OK	Interactive inputs: VALID, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	on-board protocol monitor latches an assertion-error LED

Lesson 208 - 19.5 - Safety and liveness properties

Theme and objective	Safety says a bad event never occurs; liveness says a requested good event eventually occurs under stated assumptions.
Complete example	`Safety: never read empty. Liveness: accepted request receives done within 16 cycles.`
Learner action	Which property is liveness?
Expected knowledge	Every accepted request eventually completes
Teaching aid	REQUEST ----------> DONE within bound no illegal state at any cycle
Lab target	bounded request-response properties
Controls / actions	request timing, response latency, and legal assumptions
Required lab evidence	proof depth or counterexample trace

Signals: CLK, REQ, BUSY, DONE, PROP_OK	Interactive inputs: REQ
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button requests always finish within a visible LED timeout window

Lesson 209 - 19.6 - Functional coverage design

Theme and objective	Functional coverage measures meaningful scenarios and crosses, not merely elapsed simulation time.
Complete example	`Cover opcode, boundary length, backpressure, and opcodexbackpressure.`
Learner action	What does a coverage hole identify?
Expected knowledge	A planned scenario that was not observed
Teaching aid	SCENARIOS -> COVERPOINTS -> CROSSES -> COVERAGE CLOSURE
Lab target	a protocol coverage model
Controls / actions	opcode, length boundary, backpressure, and reset timing
Required lab evidence	coverage table with no unexplained holes

Signals: CLK, OP0, LEN_MAX, STALL, HIT	Interactive inputs: OP0, LEN_MAX, STALL
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	hardware test modes exercise each planned cover bin and report a bitmap

Lesson 210 - 19.7 - Boundary-value and overflow testing

Theme and objective	Widths, counters, pointers, and arithmetic must be tested at zero, one, maximum, rollover, and signed extremes.
Complete example	`8-bit add vectors: 0+0, 1+255, 127+1, -128-1.`
Learner action	Which case exposes unsigned rollover?
Expected knowledge	255 + 1
Teaching aid	MIN - NORMAL - MAX - ROLLOVER check result, carry, overflow separately
Lab target	an arithmetic boundary regression
Controls / actions	minimum, maximum, signed edge, and rollover operands
Required lab evidence	result/carry/overflow comparison table

Signals: CLK, A_MAX, B_ONE, Y_ZERO, CARRY, OVF	Interactive inputs: A_MAX, B_ONE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch-selected boundary vectors printed with flags over UART

Lesson 211 - 19.8 - Fault injection and error observability

Theme and objective	Controlled faults prove that checkers detect corruption and that diagnostics point to the failing requirement.
Complete example	`Flip one stored bit after write; parity checker must flag the next read.`
Learner action	What validates the checker?
Expected knowledge	A known injected fault produces the expected alarm
Teaching aid	GOOD DATA -> FAULT MASK XOR -> CORRUPTED DATA -> CHECKER -> ALARM
Lab target	a parity fault-injection path
Controls / actions	fault enable, bit index, and read timing
Required lab evidence	detected fault location and alarm latency

Signals: CLK, FAULT, BIT0, PARITY_ERR, ALARM	Interactive inputs: FAULT, BIT0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button injects corruption and dedicated error LED asserts

Lesson 212 - 19.9 - Formal counterexamples and assumptions

Theme and objective	Formal tools exhaustively explore behavior under assumptions; a counterexample is a concrete trace that violates a property.
Complete example	`Assume legal reset release; assert FIFO count never exceeds DEPTH.`
Learner action	What should be done with an assumption?
Expected knowledge	Review that it constrains only the real environment
Teaching aid	ASSUMPTIONS + RTL + PROPERTY -> PROOF or COUNTEREXAMPLE
Lab target	a bounded FIFO safety proof
Controls / actions	legal write/read sequences and reset assumptions
Required lab evidence	proof result plus reviewed counterexample when intentionally broken

Signals: CLK, WRITE, READ, COUNT_OK, PROOF	Interactive inputs: WRITE, READ
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	proved safety property paired with an on-board FIFO stress test

Lesson 213 - 19.10 - Regression and verification closure

Theme and objective	Closure requires stable regressions, met coverage goals, reviewed waivers, clean assertions, and hardware acceptance evidence.
Complete example	`Run lint, unit tests, integration tests, assertions, coverage, synthesis, timing, then board acceptance.`
Learner action	Which item may be silently ignored?
Expected knowledge	None; every failure and waiver needs disposition
Teaching aid	LINT -> SIM -> ASSERT -> COVER -> IMPLEMENT -> BOARD one reproducible regression
Lab target	an automated verification closure run
Controls / actions	fixed seed set, tool settings, and board acceptance sequence
Required lab evidence	signed closure report and archived artifacts

Signals: CLK, RUN, SIM_OK, TIMING_OK, BOARD_OK	Interactive inputs: RUN
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	one command regenerates programming image and the board self-test passes

20 - High-Speed I/O and Transceivers

Bring up serial links and measure their integrity on supported hardware.

Lesson 214 - 20.1 - Parallel-to-serial data flow

Theme and objective	A serializer converts a parallel word into timed serial symbols; a deserializer rebuilds aligned parallel words.
Complete example	`8-bit word 10110010 -> serializer -> one bit per unit interval -> deserializer`
Learner action	What must the receiver recover before presenting words?
Expected knowledge	Bit timing and word alignment
Teaching aid	WORD[7:0] -> SER -> differential lane -> DES -> WORD[7:0]
Lab target	a low-rate serializer loopback
Controls / actions	parallel pattern, bit order, and word-alignment marker
Required lab evidence	transmitted/received word comparison and error count

Signals: CLK, START, TX_BIT, RX_BIT, WORD_OK	Interactive inputs: START
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	physical or internal loopback returns every test word without error

Lesson 215 - 20.2 - Differential signaling and termination

Theme and objective	High-speed differential links use a voltage difference between a pair and require compatible standards, pin pairs, and termination.
Complete example	`TX_P/TX_N drive a matched differential pair; RX compares P against N.`
Learner action	Why must P and N use a defined differential pair?
Expected knowledge	The I/O hardware and board routing are pair-specific
Teaching aid	TX_P ============= RX_P TX_N ============= RX_N matched pair + termination
Lab target	a constrained differential test output
Controls / actions	I/O standard, legal pin pair, and toggle rate
Required lab evidence	clean implementation report and measured complementary pair

Signals: CLK, ENABLE, TX_P, TX_N, PAIR_OK	Interactive inputs: ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	scope capture or receiver status verifies the differential pair

Lesson 216 - 20.3 - Reference clocks and jitter budget

Theme and objective	A transceiver reference clock must meet supported frequency and jitter limits because it anchors transmit and receive timing.
Complete example	`reference oscillator -> transceiver PLL -> serial line rate clocks`
Learner action	What can excess reference-clock jitter reduce?
Expected knowledge	The available serial sampling margin
Teaching aid	REFCLK -> PLL -> TX CLOCK +> RX/CDR support frequency + jitter budget
Lab target	a reference-clock qualification check
Controls / actions	selected reference source, divider, and lock timeout
Required lab evidence	frequency, lock status, and jitter-budget worksheet

Signals: CLK, REFSEL, PLL_LOCK, CLK_OK	Interactive inputs: REFSEL
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	SmartDebug reports stable transceiver PLL lock

Lesson 217 - 20.4 - Clock and data recovery

Theme and objective	The receiver CDR follows transition timing in the incoming serial stream and produces a recovered clock and data.
Complete example	`transition-rich serial data -> CDR -> recovered bits; long runs may require line coding or scrambling.`
Learner action	Why are transitions important?
Expected knowledge	They provide timing information to the CDR
Teaching aid	SERIAL DATA -> CDR -+> RECOVERED CLOCK +> RECOVERED DATA
Lab target	a CDR lock and loss monitor
Controls / actions	transition pattern and signal-present control
Required lab evidence	lock acquisition time and loss-of-lock indication

Signals: CLK, SIGNAL, CDR_LOCK, RX_VALID	Interactive inputs: SIGNAL
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	receiver lock LED and SmartDebug lock history

Lesson 218 - 20.5 - Line coding and disparity control

Theme and objective	A line code can limit run length, provide control symbols, and manage DC disparity at the cost of encoding overhead.
Complete example	`8b/10b maps each data byte or control character to a ten-bit transmission symbol.`
Learner action	What is the payload efficiency of 8b/10b?
Expected knowledge	80 percent
Teaching aid	8 DATA BITS -> ENCODER -> 10 LINE BITS control symbols + transition density
Lab target	an encoder/decoder symbol checker
Controls / actions	data byte, control/data selection, and error injection
Required lab evidence	decoded byte, code error, and disparity error

Signals: CLK, KCHAR, DATA0, CODE_ERR, DISP_ERR, DECODE_OK	Interactive inputs: KCHAR, DATA0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	loopback symbol test reports zero code/disparity errors

Lesson 219 - 20.6 - Word alignment and comma detection

Theme and objective	A receiver searches the serial bit stream for a defined alignment symbol, then fixes parallel word boundaries.
Complete example	`Detect comma -> slip gearbox if needed -> assert aligned -> deliver words.`
Learner action	When may payload checking begin?
Expected knowledge	After stable word alignment is established
Teaching aid	BITS -> COMMA DETECT -> BIT SLIP -> ALIGNED WORDS
Lab target	a word-alignment controller
Controls / actions	comma insertion, bit offset, and reacquisition request
Required lab evidence	alignment latency and correct payload words

Signals: CLK, COMMA, SLIP, ALIGNED, WORD_OK	Interactive inputs: COMMA, SLIP
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	forced misalignment automatically reacquires and restores link-good LED

Lesson 220 - 20.7 - Multi-lane deskew and bonding

Theme and objective	Parallel serial lanes may arrive with different delay; deskew buffers align marked blocks before combining them.
Complete example	`lane markers enter elastic buffers; bonded output releases only when all lanes align.`
Learner action	What absorbs lane-to-lane delay?
Expected knowledge	Per-lane elastic buffers
Teaching aid	LANE0 -> BUFFER -+ LANE1 -> BUFFER -+-> BONDED DATA LANE2 -> BUFFER -+
Lab target	a lane-bonding deskew model
Controls / actions	lane delay offsets and alignment markers
Required lab evidence	deskew depth, bonded-valid, and ordered data

Signals: CLK, MARK0, MARK1, DESKEW, BONDED	Interactive inputs: MARK0, MARK1
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	available transceiver lanes reach bonded-ready with reported skew

Lesson 221 - 20.8 - PRBS generation and BER measurement

Theme and objective	A pseudo-random binary sequence stresses a link; the receiver compares the expected sequence and counts bit errors over time.
Complete example	`PRBS generator -> link -> PRBS checker; BER = error bits / observed bits.`
Learner action	What does a zero error count prove?
Expected knowledge	No errors occurred during that test interval and configuration
Teaching aid	PRBS GEN -> LINK -> PRBS CHECK +> BITS +> ERRORS
Lab target	a PRBS link quality monitor
Controls / actions	pattern select, run duration, and error injection
Required lab evidence	observed bits, errors, and calculated BER bound

Signals: CLK, RUN, INJECT, LOCK, ERROR	Interactive inputs: RUN, INJECT
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	hardware PRBS run exports duration, bit count, and error count

Lesson 222 - 20.9 - Eye margin and equalization concepts

Theme and objective	An eye diagram summarizes sampling margin. Equalization compensates channel loss but must be tuned using measured results.
Complete example	`Sweep sampling phase and threshold; mark passing region; choose center margin.`
Learner action	Where is the preferred sample point?
Expected knowledge	Near the center of the stable eye opening
Teaching aid	voltage ^ _____ | / EYE \ +--/_____\--> time sample center
Lab target	an eye-margin sweep exercise
Controls / actions	sampling phase, threshold, and equalization setting
Required lab evidence	pass/fail eye map and chosen operating point

Signals: CLK, SWEEP, EQSEL, MARGIN_OK, LINK_OK	Interactive inputs: SWEEP, EQSEL
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	SmartDebug eye/diagnostic capture where supported, with selected margin setting

Lesson 223 - 20.10 - Transceiver bring-up capstone

Theme and objective	Disciplined bring-up checks power, reference clock, reset order, PLL/CDR lock, alignment, PRBS, payload, and recovery separately.
Complete example	`Bring up one loopback lane; prove locks; run PRBS; send framed payload; force and recover one fault.`
Learner action	What should be checked before payload errors?
Expected knowledge	Reference clocks, resets, locks, and alignment
Teaching aid	REFCLK -> RESET -> LOCK -> ALIGN -> PRBS -> PAYLOAD -> RECOVERY
Lab target	a measured serial-link loopback
Controls / actions	line rate, loopback mode, pattern, and forced loss-of-lock
Required lab evidence	bring-up checklist, BER run, payload match, and recovery time

Signals: CLK, RESET, PLL_LOCK, ALIGNED, DATA_OK, ERROR	Interactive inputs: RESET, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	complete SmartDebug link report and repeatable loopback demonstration

21 - External Memory and Data Movement

Control memory, buffering, arbitration, and high-throughput transfers.

Lesson 224 - 21.1 - Synchronous SRAM controller

Theme and objective	A memory controller sequences address, write data, byte enables, and read-valid timing around the memory interface contract.
Complete example	`WRITE: present address/data + WE at edge. READ: present address, then capture data when valid.`
Learner action	Why is read-valid required?
Expected knowledge	Read data may return after a defined latency
Teaching aid	REQUEST -> ADDRESS/CONTROL -> MEMORY RESPONSE <---- DATA/VALID <-------+
Lab target	a synchronous memory transaction controller
Controls / actions	read/write, address, data, and byte enable
Required lab evidence	transaction log with expected readback

Signals: CLK, WRITE, ADDR0, WDATA0, RVALID, MATCH	Interactive inputs: WRITE, ADDR0, WDATA0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	fabric memory writes and reads back switch-selected patterns over UART

Lesson 225 - 21.2 - DDR signaling concepts

Theme and objective	Double-data-rate memory transfers on both clock edges and organizes commands, addresses, banks, strobes, and data buses.
Complete example	`One clock cycle contains a rising-edge transfer and a falling-edge transfer.`
Learner action	How many transfer opportunities occur per clock cycle?
Expected knowledge	Two
Teaching aid	CLK _/-_/-_ DQ A B C D transfers at both edges
Lab target	a DDR edge-transfer teaching model
Controls / actions	edge select, burst enable, and data pattern
Required lab evidence	edge-by-edge word sequence and strobe relationship

Signals: CLK, ENABLE, DQS, DQ0, EDGE_OK	Interactive inputs: ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit DDR controller test reports passing edge-aligned transfers

Lesson 226 - 21.3 - Memory controller initialization and training

Theme and objective	External DDR cannot serve traffic until reset, initialization, calibration, and training complete successfully.
Complete example	`power stable -> reset sequence -> initialization -> training -> READY`
Learner action	When may application requests begin?
Expected knowledge	After the controller asserts READY
Teaching aid	POWER -> RESET -> INIT -> TRAIN -> READY -> TRAFFIC
Lab target	a memory-startup state machine
Controls / actions	reset, simulated training delay, and injected training failure
Required lab evidence	state trace, READY time, and failure code

Signals: CLK, START, FAIL, READY, ERROR	Interactive inputs: START, FAIL, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DDR initialization status and memory test result printed at boot

Lesson 227 - 21.4 - Burst transfers and address alignment

Theme and objective	Burst traffic amortizes command overhead by moving consecutive beats from an aligned starting address.
Complete example	`Burst length 4 from aligned address 0x20 transfers 0x20, 0x24, 0x28, 0x2C for 32-bit beats.`
Learner action	What follows address 0x24 in this burst?
Expected knowledge	0x28
Teaching aid	CMD [ADDR,LEN] -> BEAT0 -> BEAT1 -> BEAT2 -> BEAT3
Lab target	an aligned burst address generator
Controls / actions	base address, beat size, burst length, and backpressure
Required lab evidence	address sequence, beat count, and completion response

Signals: CLK, START, READY, LAST, ALIGN_OK	Interactive inputs: START, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	UART dumps a verified burst written to and read from DDR4

Lesson 228 - 21.5 - Multi-master arbitration

Theme and objective	An arbiter grants one requester at a time according to a documented fairness and priority policy.
Complete example	`Round-robin rotates priority after each accepted transaction.`
Learner action	What should a fair arbiter prevent?
Expected knowledge	Indefinite starvation of an active requester
Teaching aid	REQ0 -+ REQ1 -+-> ARBITER -> GRANT + MEMORY PORT REQ2 -+
Lab target	a three-requester round-robin arbiter
Controls / actions	request combinations and downstream ready
Required lab evidence	grant order, wait cycles, and starvation bound

Signals: CLK, REQ0, REQ1, READY, GNT0, GNT1	Interactive inputs: REQ0, REQ1, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	three fabric traffic generators report fair grant counts over UART

Lesson 229 - 21.6 - DMA descriptor engine

Theme and objective	A DMA engine moves blocks without per-word processor intervention using source, destination, length, and status descriptors.
Complete example	`descriptor {src=0x1000, dst=0x2000, len=256}; DMA copies and interrupts on completion.`
Learner action	What terminates the transfer?
Expected knowledge	The programmed length reaching zero or an error
Teaching aid	DESCRIPTOR -> READ ENGINE -> FIFO -> WRITE ENGINE -> DONE
Lab target	a small descriptor-driven DMA
Controls / actions	start, length, source pattern, and destination backpressure
Required lab evidence	byte count, checksum, completion, and error status

Signals: CLK, START, READY, LAST, DONE, ERROR	Interactive inputs: START, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	fabric DMA copies a DDR buffer and software verifies its checksum

Lesson 230 - 21.7 - Elastic buffering and rate matching

Theme and objective	An elastic FIFO separates producer and consumer timing while occupancy thresholds drive backpressure before overflow.
Complete example	`Producer writes every cycle; consumer stalls for four cycles; FIFO level rises then drains.`
Learner action	When should the producer stop?
Expected knowledge	When backpressure or the documented almost-full threshold asserts
Teaching aid	PRODUCER -> ELASTIC FIFO -> CONSUMER level -> almost_full -> backpressure
Lab target	a rate-matching elastic buffer
Controls / actions	producer rate, consumer stalls, and threshold
Required lab evidence	occupancy waveform with no overflow or underflow

Signals: CLK, WRITE, READ, ALMOST_FULL, EMPTY, LEVEL_OK	Interactive inputs: WRITE, READ
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button-controlled consumer stalls while UART reports safe FIFO levels

Lesson 231 - 21.8 - ECC and memory scrubbing

Theme and objective	Error-correcting codes detect and correct supported bit faults; scrubbing periodically reads, corrects, and rewrites memory.
Complete example	`Inject one data-bit error -> ECC corrects read -> scrubber rewrites corrected word.`
Learner action	What should happen after a correctable error?
Expected knowledge	Return corrected data and record/correct the stored location
Teaching aid	MEMORY -> ECC CHECK -+> CORRECTED DATA +> SCRUB WRITEBACK + LOG
Lab target	an SEC-DED fault and scrub model
Controls / actions	fault enable, bit location, scrub interval, and read address
Required lab evidence	corrected count, uncorrectable alarm, and data match

Signals: CLK, INJECT, SCRUB, CORRECTED, UNCORR, DATA_OK	Interactive inputs: INJECT, SCRUB
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	injected single-bit fault increments correction counter without data mismatch

Lesson 232 - 21.9 - Bandwidth, latency, and efficiency

Theme and objective	Measured memory performance separates first-response latency, sustained bandwidth, protocol overhead, and idle cycles.
Complete example	`Efficiency = transferred data beats / available beat slots during the measurement window.`
Learner action	What improves burst efficiency?
Expected knowledge	Longer legal bursts with fewer idle gaps
Teaching aid	REQUEST - latency -> FIRST DATA - sustained beats -> DONE measure cycles, bytes, and stalls
Lab target	a hardware performance counter set
Controls / actions	burst length, outstanding requests, and backpressure
Required lab evidence	cycles, bytes, latency, bandwidth, and utilization

Signals: CLK, RUN, VALID, READY, LAST, PERF_OK	Interactive inputs: RUN, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DDR benchmark prints measured latency and MB/s over UART

Lesson 233 - 21.10 - Memory-to-streaming capstone

Theme and objective	A complete data mover reads burst data, buffers it, applies backpressure, transforms each word, and writes results with end-to-end checks.
Complete example	`DDR source -> read DMA -> FIFO -> XOR transform -> write DMA -> DDR destination.`
Learner action	Where should backpressure be absorbed?
Expected knowledge	By the FIFO and handshake logic without losing order
Teaching aid	DDR READ -> DMA -> FIFO -> TRANSFORM -> DMA -> DDR WRITE scoreboard checks every word
Lab target	an end-to-end DDR data mover
Controls / actions	buffer addresses, length, transform key, and forced stalls
Required lab evidence	matching destination buffer, throughput, timing, and utilization reports

Signals: CLK, START, STALL, VALID, LAST, DONE, ERROR	Interactive inputs: START, STALL, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit DDR-to-DDR transfer passes software checksum and reports throughput

22 - PolarFire SoC and RISC-V Integration

Connect FPGA fabric with the PolarFire SoC microprocessor subsystem.

Lesson 234 - 22.1 - MSS and FPGA fabric partitioning

Theme and objective	PolarFire SoC combines a hardened RISC-V microprocessor subsystem with programmable FPGA fabric; partition by latency, parallelism, flexibility, and software needs.
Complete example	`Linux configures thresholds; fabric samples inputs and evaluates them every cycle.`
Learner action	Which work best fits fabric?
Expected knowledge	Deterministic parallel signal processing
Teaching aid	RISC-V MSS <-> memory-mapped bridge <-> FPGA FABRIC software control parallel hardware
Lab target	a hardware/software partition diagram
Controls / actions	software command, fabric input, and status response
Required lab evidence	partition rationale and measured response latency

Signals: CLK, CMD, INPUT, STATUS, IRQ	Interactive inputs: CMD, INPUT
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Linux or bare-metal command controls a fabric LED function

Lesson 235 - 22.2 - Memory maps and address decoding

Theme and objective	A memory map assigns non-overlapping address ranges to control, status, memory, and peripheral blocks.
Complete example	`0x6000_0000 CONTROL; 0x6000_0004 STATUS; low address bits select registers.`
Learner action	What must two peripheral ranges avoid?
Expected knowledge	Address overlap
Teaching aid	CPU ADDRESS -> RANGE DECODE -+> CONTROL REG +> STATUS REG
Lab target	a fabric register address decoder
Controls / actions	address, read/write, write data, and invalid address
Required lab evidence	readback table and decode-error response

Signals: CLK, WRITE, ADDR0, WDATA0, RDATA0, ERROR	Interactive inputs: WRITE, ADDR0, WDATA0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	SoftConsole reads and writes documented fabric addresses

Lesson 236 - 22.3 - APB control-register peripheral

Theme and objective	APB provides a simple setup/access transfer for low-bandwidth control and status peripherals.
Complete example	`Setup selects address; access asserts PENABLE; peripheral returns PREADY and optional PSLVERR.`
Learner action	When does an APB transfer complete?
Expected knowledge	During access with PSEL, PENABLE, and PREADY asserted
Teaching aid	SETUP: PSEL + address ACCESS: PENABLE + PREADY -> complete
Lab target	an APB LED and switch peripheral
Controls / actions	PSEL, PENABLE, write/read, address, and wait state
Required lab evidence	protocol assertion log and register readback

Signals: CLK, PSEL, PENABLE, PWRITE, PREADY, PSLVERR	Interactive inputs: PSEL, PENABLE, PWRITE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	RISC-V software writes LED register and reads DIP-switch status

Lesson 237 - 22.4 - AXI-style ready-valid channels

Theme and objective	AXI channels transfer only when VALID and READY meet; payload must remain stable while stalled.
Complete example	`Master holds address and VALID until slave raises READY.`
Learner action	What must remain stable during backpressure?
Expected knowledge	The channel payload while VALID is high
Teaching aid	VALID + PAYLOAD -----> <---- READY transfer at VALID && READY
Lab target	a backpressure-safe streaming bridge
Controls / actions	VALID, READY, payload, and random stalls
Required lab evidence	no lost/duplicated transfers and stable-payload assertions

Signals: CLK, VALID, READY, DATA, LAST, ERROR	Interactive inputs: VALID, READY, DATA
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	fabric stream counter matches software-sent transaction count

Lesson 238 - 22.5 - Interrupt generation and service

Theme and objective	A fabric interrupt records an event, asserts a request, and remains observable until software acknowledges or clears it.
Complete example	`event sets pending; IRQ rises; handler reads cause and writes clear; IRQ falls.`
Learner action	Why latch the pending event?
Expected knowledge	A short event must remain visible until software handles it
Teaching aid	EVENT -> PENDING -> IRQ -> RISC-V HANDLER -> CLEAR
Lab target	a latched fabric interrupt source
Controls / actions	event pulse, mask, clear, and repeated event timing
Required lab evidence	interrupt count, cause, latency, and clear behavior

Signals: CLK, EVENT, MASK, IRQ, CLEAR, PENDING	Interactive inputs: EVENT, MASK, CLEAR
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button-generated fabric interrupt logged by SoftConsole

Lesson 239 - 22.6 - Fabric DMA and shared buffers

Theme and objective	DMA moves bulk data between fabric and memory while software manages descriptors, ownership, and completion.
Complete example	`software fills descriptor -> fabric DMA runs -> completion interrupt -> software verifies checksum.`
Learner action	What prevents simultaneous ownership?
Expected knowledge	A documented descriptor and buffer ownership protocol
Teaching aid	SOFTWARE BUFFER <-> DMA <-> FABRIC STREAM ownership flag + completion interrupt
Lab target	a shared-buffer DMA transaction
Controls / actions	descriptor start, length, ownership, and stalls
Required lab evidence	checksum, byte count, completion IRQ, and ownership trace

Signals: CLK, START, OWNED, VALID, DONE, IRQ	Interactive inputs: START, OWNED
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	DDR buffer processed by fabric and verified by RISC-V software

Lesson 240 - 22.7 - Clock and reset boundaries in an SoC

Theme and objective	MSS and fabric peripherals may use different clocks and reset sequences; bridges must not transfer until both sides are ready.
Complete example	`MSS reset release + fabric PLL lock + bridge reset synchronizers -> bridge_ready.`
Learner action	When may the bridge accept traffic?
Expected knowledge	After both clock domains and reset sequences are ready
Teaching aid	MSS_READY -+ FABRIC_READY -+-> BRIDGE_READY -> transactions PLL_LOCK -----+
Lab target	a cross-domain bridge startup controller
Controls / actions	MSS ready, fabric lock, reset, and early request
Required lab evidence	no transfer before ready and deterministic restart

Signals: CLK, MSS_OK, PLL_LOCK, BRIDGE_OK, REQUEST, ERROR	Interactive inputs: MSS_OK, REQUEST, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	power-cycle log proves fabric peripheral is safe before software access

Lesson 241 - 22.8 - Bare-metal driver development

Theme and objective	A bare-metal driver defines register offsets, masks, ordering, timeouts, and error returns for one hardware peripheral.
Complete example	`write CONTROL.START; poll STATUS.DONE with timeout; read RESULT; clear DONE.`
Learner action	Why include a timeout?
Expected knowledge	Software must recover if hardware never completes
Teaching aid	DRIVER API -> CONTROL REG -> HARDWARE -> STATUS/RESULT -> DRIVER
Lab target	a C driver for a fabric arithmetic engine
Controls / actions	operation, operands, start, timeout, and error injection
Required lab evidence	driver test transcript and correct hardware result

Signals: CLK, START, OP0, DONE, TIMEOUT, RESULT	Interactive inputs: START, OP0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	SoftConsole bare-metal application runs ten hardware vectors

Lesson 242 - 22.9 - Linux device-tree and userspace access

Theme and objective	Linux needs a device-tree description and a suitable driver or controlled userspace interface to locate fabric peripherals.
Complete example	`Device-tree node declares compatible string, register range, and interrupt.`
Learner action	What does the reg property describe?
Expected knowledge	The peripheral address range
Teaching aid	DEVICE TREE -> DRIVER/BINDING -> /dev or sysfs -> APPLICATION
Lab target	a Linux-visible fabric status peripheral
Controls / actions	device-tree base address, range, interrupt, and access permissions
Required lab evidence	boot binding message and controlled read/write transcript

Signals: CLK, ENABLE, STATUS, IRQ, ACCESS_OK	Interactive inputs: ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit Linux reads switch state and controls a fabric LED

Lesson 243 - 22.10 - Hardware-software acceleration capstone

Theme and objective	A useful accelerator has a measured baseline, explicit data movement, correct control/status, interrupts, verification, and board performance evidence.
Complete example	`Software CRC baseline -> DMA buffer to fabric CRC -> completion IRQ -> compare result and execution time.`
Learner action	What determines real acceleration benefit?
Expected knowledge	End-to-end measured time including data movement and control
Teaching aid	SOFTWARE -> BUFFER/DMA -> FABRIC ACCELERATOR -> IRQ/RESULT compare correctness + end-to-end time
Lab target	a fabric CRC or checksum accelerator
Controls / actions	buffer size, seed, DMA mode, and injected mismatch
Required lab evidence	matching result, latency, throughput, CPU use, and timing report

Signals: CLK, START, VALID, LAST, DONE, MATCH	Interactive inputs: START, VALID, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit software reports hardware/software result and speed comparison

23 - Power, Thermal, and Reliability Engineering

Measure and improve power efficiency, robustness, and recoverability.

Lesson 244 - 23.1 - Static and dynamic power

Theme and objective	Total device power includes static leakage and dynamic switching power from clocks, logic, memories, I/O, and transceivers.
Complete example	`Dynamic power rises with activity, capacitance, voltage squared, and frequency.`
Learner action	Which change usually lowers dynamic power?
Expected knowledge	Reducing unnecessary switching activity
Teaching aid	TOTAL POWER = STATIC + CLOCK + LOGIC + RAM + I/O + XCVR
Lab target	an activity-controlled toggle bank
Controls / actions	enable, toggle density, and clock rate
Required lab evidence	power-estimator comparison and measured current trend

Signals: CLK, ENABLE, ACTIVITY, CLOCK_ON, POWER_OK	Interactive inputs: ENABLE, ACTIVITY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	two activity modes compared with board current monitor or estimator

Lesson 245 - 23.2 - Clock enable instead of fabric gating

Theme and objective	Use synchronous clock enables for ordinary state control so dedicated clock resources remain intact and timing stays analyzable.
Complete example	`always_ff @(posedge clk) if (enable) count <= count + 1;`
Learner action	What happens while enable is zero?
Expected knowledge	The register holds while the clock network remains valid
Teaching aid	GLOBAL CLK -> FF ENABLE ------> CE input; state holds when CE=0
Lab target	an enabled counter bank
Controls / actions	clock enable duty cycle and counter load
Required lab evidence	correct hold behavior and lower activity estimate

Signals: CLK, ENABLE, COUNT0, HOLD_OK, ACTIVITY	Interactive inputs: ENABLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	switch enable freezes LED count without altering the global clock

Lesson 246 - 23.3 - Operand isolation

Theme and objective	Operand isolation holds or masks inputs to an inactive combinational block so internal nodes do not toggle uselessly.
Complete example	`mult_a = active ? a : 0; mult_b = active ? b : 0;`
Learner action	What is preserved when active is zero?
Expected knowledge	Functional inactivity with reduced internal switching
Teaching aid	A,B -> ISOLATION -> DSP BLOCK -> RESULT ACTIVE controls switching
Lab target	an isolated arithmetic datapath
Controls / actions	active duty cycle and changing operands
Required lab evidence	identical active results and reduced toggle count while idle

Signals: CLK, ACTIVE, A0, B0, RESULT, TOGGLE	Interactive inputs: ACTIVE, A0, B0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	UART activity counter compares isolated and non-isolated modes

Lesson 247 - 23.4 - Efficient memory and DSP mapping

Theme and objective	Dedicated RAM and math blocks usually provide better density, performance, and power than equivalent distributed logic when templates match.
Complete example	`A pipelined multiply-accumulate maps to a math block; a deep synchronous array maps to LSRAM.`
Learner action	What confirms the intended mapping?
Expected knowledge	The synthesis resource report
Teaching aid	RTL TEMPLATE -> SYNTHESIS -+> MATH BLOCK +> LSRAM
Lab target	a RAM-fed multiply-accumulate kernel
Controls / actions	memory depth, coefficient, enable, and pipeline rate
Required lab evidence	resource mapping, timing, result, and activity reports

Signals: CLK, ENABLE, DATA0, COEF0, VALID, RESULT	Interactive inputs: ENABLE, DATA0, COEF0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	mapped math/RAM resources process switch-seeded samples and print results

Lesson 248 - 23.5 - I/O and transceiver power states

Theme and objective	I/O standards, toggle rates, termination, and transceiver power states can dominate interface power and must follow device guidance.
Complete example	`Disable or place an unused lane into its supported low-power state instead of transmitting idle noise.`
Learner action	What should guide an I/O power choice?
Expected knowledge	Electrical requirements plus measured or estimated power
Teaching aid	ACTIVE LINK -> NORMAL STATE INACTIVE LINK -> supported low-power state -> wake sequence
Lab target	an interface activity and sleep controller
Controls / actions	enable, idle timeout, wake request, and link lock
Required lab evidence	state transitions, wake latency, and power comparison

Signals: CLK, ENABLE, IDLE, SLEEP, LOCK, READY	Interactive inputs: ENABLE, IDLE
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire Evaluation Kit or PolarFire Splash Kit
BOARD EVIDENCE	link state and lock recovery captured with corresponding power estimate

Lesson 249 - 23.6 - Power estimation with realistic activity

Theme and objective	A useful power estimate needs the exact device, implemented resources, clock frequencies, I/O settings, and representative toggle activity.
Complete example	`Import post-implementation activity or enter measured rates; compare worst-case and typical scenarios.`
Learner action	Why is a default toggle rate risky?
Expected knowledge	It may not represent the real workload
Teaching aid	IMPLEMENTED DESIGN + CLOCKS + I/O + ACTIVITY -> POWER ESTIMATE
Lab target	a two-scenario power-estimation study
Controls / actions	idle/active activity files, temperature, and voltage assumptions
Required lab evidence	documented typical and worst-case rail estimates

Signals: CLK, MODE, ACTIVITY, EST_OK, TEMP_OK	Interactive inputs: MODE, ACTIVITY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	estimator inputs archived and compared with available board rail readings

Lesson 250 - 23.7 - Thermal budget and junction temperature

Theme and objective	Junction temperature depends on ambient conditions, power, airflow, board, package, and thermal path; the design must retain margin.
Complete example	`Estimate Tj from tool/package model, then validate under representative workload and ambient.`
Learner action	Which temperature matters for device limits?
Expected knowledge	Junction temperature
Teaching aid	POWER + AMBIENT + THERMAL PATH -> JUNCTION TEMPERATURE + MARGIN
Lab target	a workload thermal-margin monitor
Controls / actions	activity mode, duty cycle, ambient assumption, and alarm threshold
Required lab evidence	estimated/measured temperature and remaining margin

Signals: CLK, MODE, LOAD, TEMP_ALARM, MARGIN_OK	Interactive inputs: MODE, LOAD
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	sustained workload log with rail/current data and temperature estimate

Lesson 251 - 23.8 - Synchronizer MTBF reasoning

Theme and objective	Synchronizer reliability improves with available resolution time and degrades as source transitions and destination frequency increase.
Complete example	`Compare one-stage and two-stage synchronizers using the device metastability guidance and real clock/event rates.`
Learner action	Which change usually improves synchronizer MTBF?
Expected knowledge	Adding settling time before the synchronized value is consumed
Teaching aid	ASYNC EVENT -> FF1 - resolution time -> FF2 -> SAFE LOGIC
Lab target	a synchronizer reliability worksheet and implementation
Controls / actions	source event rate, destination frequency, and stage count
Required lab evidence	documented MTBF rationale and clean CDC structure

Signals: CLK, ASYNC, FF1, FF2, SAFE	Interactive inputs: ASYNC
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	implemented synchronizer plus CDC report and measured event-rate assumptions

Lesson 252 - 23.9 - Watchdogs, fault detection, and recovery

Theme and objective	A robust design detects stalled progress, records the cause, moves outputs safe, and attempts only a controlled recovery.
Complete example	`Heartbeat must change before timeout; otherwise latch fault, force safe output, reset subsystem.`
Learner action	What should survive recovery?
Expected knowledge	A diagnostic indication of the fault cause when required
Teaching aid	HEARTBEAT -> WATCHDOG - timeout -> SAFE STATE + FAULT LOG + RESET
Lab target	a recoverable subsystem watchdog
Controls / actions	heartbeat stop, timeout value, acknowledge, and repeat fault
Required lab evidence	detection latency, safe output, cause code, and recovery count

Signals: CLK, HEARTBEAT, STALL, FAULT, SAFE, RECOVERED	Interactive inputs: HEARTBEAT, STALL, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	button stalls heartbeat; fault LED and automatic recovery behave as specified

Lesson 253 - 23.10 - Low-power reliable subsystem capstone

Theme and objective	A production-quality subsystem balances power, performance, temperature, CDC reliability, fault detection, and measurable recovery.
Complete example	`Sensor pipeline sleeps when idle, wakes on event, processes in DSP/RAM, reports result, and recovers from an injected stall.`
Learner action	What is the final acceptance basis?
Expected knowledge	Correct function plus measured power, timing, thermal, and recovery evidence
Teaching aid	EVENT -> WAKE -> PROCESS -> REPORT -> IDLE fault -> SAFE -> RECOVER
Lab target	a power-managed reliable sensor pipeline
Controls / actions	event rate, active mode, idle timeout, and injected stall
Required lab evidence	functional, timing, power, thermal, CDC, and recovery report set

Signals: CLK, EVENT, ACTIVE, DONE, FAULT, SLEEP, RECOVERED	Interactive inputs: EVENT, ACTIVE, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit demonstrates sleep/wake, result UART, fault alarm, and recovery

24 - FPGA Security and Provisioning

Protect configuration, debug access, keys, and the device lifecycle.

Lesson 254 - 24.1 - Threat modeling the FPGA system

Theme and objective	A threat model identifies assets, trust boundaries, attackers, attack surfaces, impacts, and mitigations before security settings are chosen.
Complete example	`Assets: RTL IP and keys. Surfaces: programming file, JTAG, boot storage, debug port, external bus.`
Learner action	What comes before selecting a mitigation?
Expected knowledge	Identify the asset and credible threat
Teaching aid	ASSETS -> TRUST BOUNDARIES -> THREATS -> MITIGATIONS -> TESTS
Lab target	a board-specific threat model
Controls / actions	attacker capability, exposed interface, and protected asset
Required lab evidence	reviewed threat/mitigation/test matrix

Signals: CLK, DEBUG, PROGRAM, ALERT, ACCESS_OK	Interactive inputs: DEBUG, PROGRAM
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit interface inventory and security acceptance checklist

Lesson 255 - 24.2 - Programming image authentication

Theme and objective	Authentication lets the device reject a modified or unauthorized programming image before trusting it.
Complete example	`Verify image authenticity/integrity -> accept and program, otherwise reject and log failure.`
Learner action	What does authentication primarily prove?
Expected knowledge	The image is authorized and has not been altered undetected
Teaching aid	IMAGE + AUTHENTICATOR -> VERIFY -+> ACCEPT +> REJECT
Lab target	an authenticated-update state model
Controls / actions	valid image, modified image, version, and retry
Required lab evidence	accept/reject result and failure reason

Signals: CLK, START, IMAGE_OK, ACCEPT, REJECT	Interactive inputs: START, IMAGE_OK, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	documented programming flow accepts approved image and rejects a safe invalid test artifact

Lesson 256 - 24.3 - Configuration confidentiality

Theme and objective	Encryption protects programming-image contents, while authentication separately protects origin and integrity; a secure flow normally needs both.
Complete example	`encrypted + authenticated image travels through controlled storage and programming tools.`
Learner action	What does encryption not replace?
Expected knowledge	Authentication of the image
Teaching aid	PLAINTEXT DESIGN -> AUTH + ENCRYPT -> PROTECTED IMAGE -> DEVICE
Lab target	a protected-image lifecycle diagram
Controls / actions	image state, authorized operation, and invalid-tag case
Required lab evidence	asset-flow review and protected artifact inventory

Signals: CLK, LOAD, TAG_OK, DECRYPT_OK, FAULT	Interactive inputs: LOAD, TAG_OK
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	controlled FlashPro/Libero programming record with no keys stored in the app

Lesson 257 - 24.4 - Root keys and key hierarchy

Theme and objective	A key hierarchy limits exposure by deriving or wrapping purpose-specific keys from a protected root rather than reusing one key everywhere.
Complete example	`root trust -> image key, update key, data key; rotate a child without replacing the root.`
Learner action	Where should plaintext secret keys be avoided?
Expected knowledge	Source control, logs, and lesson artifacts
Teaching aid	ROOT OF TRUST -+> IMAGE KEY +> UPDATE KEY +> DATA KEY
Lab target	a non-secret key hierarchy exercise
Controls / actions	key purpose, owner, storage boundary, and rotation event
Required lab evidence	key inventory containing identifiers but no key material

Signals: CLK, REQUEST, POLICY_OK, KEY_VALID, DENY	Interactive inputs: REQUEST, POLICY_OK
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	provisioning worksheet and device policy demonstration using non-secret training identifiers

Lesson 258 - 24.5 - Secure boot and measured startup

Theme and objective	A secure startup chain verifies each executable stage before transferring control and reports failure without running untrusted code.
Complete example	`immutable trust anchor -> verify first stage -> verify next stage -> start application.`
Learner action	What preserves the chain of trust?
Expected knowledge	Every stage verifies the next before execution
Teaching aid	ROOT -> VERIFY STAGE1 -> VERIFY STAGE2 -> APPLICATION failure -> SAFE/RECOVERY
Lab target	a secure-startup controller model
Controls / actions	stage-valid bits, rollback policy, and failure injection
Required lab evidence	startup state, accepted version, and rejection reason

Signals: CLK, BOOT, STAGE1_OK, STAGE2_OK, RUN, FAULT	Interactive inputs: BOOT, STAGE1_OK, STAGE2_OK, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit boot log records accepted stages and controlled failure behavior

Lesson 259 - 24.6 - JTAG and debug access policy

Theme and objective	Debug access is powerful and must follow a lifecycle policy that distinguishes development, manufacturing, service, and deployed states.
Complete example	`Development allows authenticated debug; deployed policy restricts unauthorized access and records service procedure.`
Learner action	Why avoid an undocumented permanent lock?
Expected knowledge	It can make authorized recovery impossible and create lifecycle risk
Teaching aid	LIFECYCLE STATE + AUTHORIZATION -> JTAG POLICY -> ALLOW / DENY / MONITOR
Lab target	a reversible training debug-policy model
Controls / actions	lifecycle state, authorized request, and failed request
Required lab evidence	policy decision and audit event

Signals: CLK, DEV_MODE, AUTH, ALLOW, DENY, ALERT	Interactive inputs: DEV_MODE, AUTH
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	non-destructive debug-policy simulation paired with documented board recovery path

Lesson 260 - 24.7 - Controlled provisioning process

Theme and objective	Provisioning assigns device identity, policy, and protected material through authorized tools with separation of duties and audit records.
Complete example	`approve job -> identify device -> apply policy/material -> verify -> archive non-secret record.`
Learner action	What belongs in the audit record?
Expected knowledge	Device/job identifiers, policy version, result, operator role, and time
Teaching aid	APPROVAL -> DEVICE ID -> PROVISION -> VERIFY -> AUDIT RECORD
Lab target	a safe provisioning workflow rehearsal
Controls / actions	job authorization, device identity, policy version, and verify failure
Required lab evidence	complete non-secret audit record and recovery decision

Signals: CLK, APPROVED, ID_OK, VERIFY_OK, COMPLETE	Interactive inputs: APPROVED, ID_OK
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	training provisioning checklist completed without exposing secret material

Lesson 261 - 24.8 - Zeroization and safe failure

Theme and objective	A zeroization policy defines which volatile or protected assets are cleared, which event authorizes it, and how the system enters a safe state.
Complete example	`validated tamper/fatal policy event -> clear designated assets -> disable sensitive function -> report state.`
Learner action	Why must zeroization be tested carefully?
Expected knowledge	It may be irreversible or remove recovery data on real hardware
Teaching aid	AUTHORIZED EVENT -> ZEROIZE SELECTED ASSETS -> SAFE STATE Use simulation/training mode unless approved
Lab target	a reversible zeroization state model
Controls / actions	training authorize, event source, cancel window, and completion
Required lab evidence	cleared training registers and safe-state indication

Signals: CLK, AUTHORIZE, EVENT, CLEARED, SAFE	Interactive inputs: AUTHORIZE, EVENT, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	reversible training registers clear and safe LED asserts; no permanent device lock

Lesson 262 - 24.9 - Runtime integrity and tamper response

Theme and objective	Runtime monitors can check configuration integrity, clock/voltage anomalies, illegal states, or enclosure signals and route policy-driven responses.
Complete example	`monitor event -> filter/confirm -> log cause -> isolate sensitive output -> alert supervisor.`
Learner action	What prevents nuisance responses?
Expected knowledge	Documented filtering, confirmation, and policy thresholds
Teaching aid	MONITORS -> QUALIFY -> LOG -> ISOLATE / ALERT / RECOVER
Lab target	a multi-source integrity monitor
Controls / actions	fault source, confirmation count, mask policy, and acknowledge
Required lab evidence	qualified cause, response latency, and recovery log

Signals: CLK, FAULT0, FAULT1, QUALIFIED, ALERT, SAFE	Interactive inputs: FAULT0, FAULT1
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	buttons emulate safe fault sources and demonstrate logged policy response

Lesson 263 - 24.10 - Secure lifecycle capstone

Theme and objective	A secure FPGA lifecycle connects threat model, image protection, key policy, boot, debug, provisioning, runtime monitoring, updates, recovery, and retirement.
Complete example	`Review one device from development through deployed update and authorized recovery without exposing secrets.`
Learner action	What is the strongest completion evidence?
Expected knowledge	A reviewed lifecycle plan plus tested authorized and rejected paths
Teaching aid	THREAT -> DESIGN -> PROVISION -> BOOT -> OPERATE -> UPDATE -> RECOVER -> RETIRE
Lab target	a complete non-destructive security lifecycle demo
Controls / actions	lifecycle mode, image status, authorization, fault, and recovery request
Required lab evidence	policy matrix, test log, audit record, and safe board demonstration

Signals: CLK, MODE, AUTH, IMAGE_OK, ALERT, RECOVERY	Interactive inputs: MODE, AUTH, IMAGE_OK, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit demonstrates authorized startup/update model and rejected invalid cases

25 - Professional FPGA Capstone

Deliver a traceable design from requirements through measured hardware.

Lesson 264 - 25.1 - Measurable requirements and acceptance criteria

Theme and objective	A strong requirement states an observable behavior, conditions, limits, and pass/fail evidence without prescribing unnecessary implementation.
Complete example	`When enabled, the system shall accept one sample per cycle at 50 MHz with no loss for bursts up to 256 samples.`
Learner action	Which phrase makes acceptance measurable?
Expected knowledge	No loss for bursts up to 256 samples at 50 MHz
Teaching aid	NEED -> MEASURABLE REQUIREMENT -> TEST METHOD -> PASS/FAIL EVIDENCE
Lab target	a capstone requirements baseline
Controls / actions	operating mode, rate, burst size, reset, error, and environment
Required lab evidence	approved requirement and acceptance matrix

Signals: CLK, ENABLE, VALID, READY, ACCEPT, ERROR	Interactive inputs: ENABLE, VALID, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	board acceptance procedure names exact switches, LEDs, UART records, and timing limits

Lesson 265 - 25.2 - Architecture and resource budgeting

Theme and objective	Architecture partitions functions into modules and budgets clocks, latency, throughput, logic, registers, RAM, DSP, I/O, and power before coding.
Complete example	`Input interface -> FIFO -> DSP pipeline -> result register -> UART monitor.`
Learner action	Why keep resource margin?
Expected knowledge	Integration and timing fixes may require additional resources
Teaching aid	INPUT -> BUFFER -> PROCESS -> OUTPUT budgets: latency, rate, LUT/FF, RAM, DSP, clocks, power
Lab target	a budgeted streaming architecture
Controls / actions	sample rate, pipeline depth, buffer depth, and device limits
Required lab evidence	block diagram and resource/latency budget table

Signals: CLK, START, VALID, READY, DONE, BUDGET_OK	Interactive inputs: START, VALID, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	selected Discovery Kit resources and peripherals traced to the architecture

Lesson 266 - 25.3 - Interface control document

Theme and objective	An interface control document defines names, widths, polarity, timing, handshakes, reset values, legal sequences, and error behavior between modules.
Complete example	`Stream: data[15:0], valid, ready, last; transfer on rising edge with valid&&ready.`
Learner action	What must be defined for backpressure?
Expected knowledge	Payload stability and transfer conditions
Teaching aid	PRODUCER [data,valid,last] -> CONSUMER PRODUCER <---------- [ready] ICD defines every cycle rule
Lab target	a reviewed streaming interface contract
Controls / actions	valid, ready, last, reset, illegal sequence, and timeout
Required lab evidence	interface table, timing diagram, and assertion list

Signals: CLK, VALID, READY, LAST, DATA0, ERROR	Interactive inputs: VALID, READY, LAST, DATA0
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	same interface drives a UART-monitored stream on the board

Lesson 267 - 25.4 - RTL implementation and review standard

Theme and objective	Capstone RTL must follow consistent rules for clocking, resets, combinational completeness, widths, parameters, CDC, hierarchy, and warnings.
Complete example	`Peer review checks one driver, explicit widths, nonblocking sequential assignments, defaults, and documented crossings.`
Learner action	When is an implementation warning acceptable?
Expected knowledge	Only after understanding, documenting, and approving its impact
Teaching aid	REQUIREMENT -> MODULE CONTRACT -> RTL -> LINT/REVIEW -> UNIT TEST
Lab target	a reviewed capstone RTL hierarchy
Controls / actions	parameters, reset, boundary data, disabled mode, and fault case
Required lab evidence	review checklist and zero unexplained warnings

Signals: CLK, ENABLE, RST, DATA0, VALID, RESULT	Interactive inputs: ENABLE, DATA0, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	reviewed source builds the board image with no unexplained warnings

Lesson 268 - 25.5 - Layered verification plan

Theme and objective	Unit tests, interface assertions, subsystem scoreboards, formal properties, integration tests, and hardware acceptance cover different failure classes.
Complete example	`Prove FIFO safety formally; simulate DSP accuracy; integrate DMA; run board throughput acceptance.`
Learner action	Why not rely only on the final board test?
Expected knowledge	Internal corner cases and failure locations are harder to isolate on hardware
Teaching aid	UNIT + ASSERT + FORMAL + SUBSYSTEM + INTEGRATION + BOARD ACCEPTANCE
Lab target	a layered capstone verification campaign
Controls / actions	normal, boundary, backpressure, reset, fault, and performance scenarios
Required lab evidence	traceable tests, assertions, coverage, and acceptance results

Signals: CLK, RUN, UNIT_OK, INTEG_OK, BOARD_OK	Interactive inputs: RUN
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	automated self-test and scripted board acceptance both pass

Lesson 269 - 25.6 - Constraints and timing closure

Theme and objective	Timing closure starts with correct clocks and I/O constraints, then uses path reports to improve architecture, pipelining, placement, and fanout.
Complete example	`Identify worst negative slack path; verify constraint; pipeline long logic; rerun all timing corners.`
Learner action	What must happen after fixing one path?
Expected knowledge	Rerun complete timing analysis because another path may become critical
Teaching aid	CONSTRAIN -> ANALYZE PATH -> ARCHITECTURAL FIX -> IMPLEMENT -> RECHECK ALL
Lab target	a timing-closed processing path
Controls / actions	target frequency, pipeline option, I/O delay, and fanout case
Required lab evidence	setup/hold reports with positive slack at required corners

Signals: CLK, START, STAGE1, STAGE2, DONE, TIMING_OK	Interactive inputs: START
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	passing Libero timing reports plus measured output rate

Lesson 270 - 25.7 - Libero implementation and programming package

Theme and objective	A reproducible hardware release records exact device, sources, constraints, IP versions, tool version, reports, programming image digest, and procedure.
Complete example	`Clean checkout -> scripted/project build -> reports -> programming image -> FlashPro programming -> verify digest.`
Learner action	What identifies the exact programmed artifact?
Expected knowledge	A versioned file plus recorded cryptographic digest
Teaching aid	SOURCE/CONSTRAINT VERSIONS -> LIBERO BUILD -> REPORTS + IMAGE + DIGEST
Lab target	a reproducible Libero release package
Controls / actions	clean build, target device, constraint set, and release identifier
Required lab evidence	manifest, reports, image digest, and programming log

Signals: CLK, BUILD, VERIFY, PROGRAM, IMAGE_OK	Interactive inputs: BUILD, VERIFY, PROGRAM
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	clean release programs a second time and reproduces identical behavior

Lesson 271 - 25.8 - Board bring-up and fault isolation

Theme and objective	Bring-up proceeds from power and clocks to reset, programming, static I/O, simple heartbeat, interfaces, memory, processing, and full workload.
Complete example	`If UART fails, first verify clock/reset and a known GPIO heartbeat before debugging protocol payload.`
Learner action	Why use staged bring-up?
Expected knowledge	It isolates faults to the earliest failing dependency
Teaching aid	POWER -> CLOCK -> RESET -> PROGRAM -> GPIO -> UART -> MEMORY -> PIPELINE
Lab target	a staged capstone board bring-up
Controls / actions	diagnostic mode, loopback, memory test, fault injection, and recovery
Required lab evidence	bring-up checklist with first-failure evidence

Signals: CLK, POWER_OK, CLK_OK, RESET_OK, LINK_OK, SYSTEM_OK	Interactive inputs: POWER_OK, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	Discovery Kit passes each staged diagnostic before full application mode

Lesson 272 - 25.9 - Performance and power measurement

Theme and objective	Final claims must use defined workloads, measurement windows, units, instrumentation, environmental conditions, and repeatable calculations.
Complete example	`Measure accepted samples and cycles for throughput; timestamp request/response for latency; record current during fixed workload.`
Learner action	What makes a benchmark comparable?
Expected knowledge	The same documented workload and measurement method
Teaching aid	WORKLOAD + WINDOW + INSTRUMENTS -> THROUGHPUT, LATENCY, POWER, EFFICIENCY
Lab target	a repeatable capstone benchmark
Controls / actions	workload size, clock, backpressure, active/idle mode, and run count
Required lab evidence	raw measurements, calculations, uncertainty, and requirement comparison

Signals: CLK, RUN, ACTIVE, VALID, READY, MEASURE_OK	Interactive inputs: RUN, ACTIVE, READY
In-app controls: clocked, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	UART benchmark log and board power/estimator record for fixed workload

Lesson 273 - 25.10 - Final portfolio demonstration

Theme and objective	The final deliverable connects requirements, architecture, RTL, tests, assertions, coverage, constraints, implementation, programming, measurements, limitations, and maintenance instructions.
Complete example	`Demonstrate reset, normal workload, boundary workload, backpressure, injected fault, recovery, throughput, and reproducible reprogramming.`
Learner action	What distinguishes a professional FPGA portfolio?
Expected knowledge	Traceable claims supported by reproducible simulation and real-board evidence
Teaching aid	REQUIREMENTS <-> DESIGN <-> VERIFICATION <-> TIMING <-> BOARD <-> MEASUREMENTS complete traceability
Lab target	the complete PolarFire board capstone
Controls / actions	all acceptance modes, boundary cases, faults, recovery, and benchmark
Required lab evidence	source package, reports, ten-test results, captures, manual, and demo checklist

Signals: CLK, RESET, START, VALID, DONE, FAULT, SYSTEM_OK	Interactive inputs: RESET, START, VALID, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT)
BOARD EVIDENCE	live Discovery Kit demonstration with archived UART, timing, utilization, and measurement evidence

26 - Real Board Project Studio

Build, simulate, constrain, and document ten original FPGA designs for the Microchip PolarFire SoC Discovery Kit.

Lesson 274 - 26.1 - Waveform and PRBS signal generator

Theme and objective	Generate square, sawtooth, triangle, and pseudo-random streams from a phase accumulator. This is an original Rintronic teaching design. Read rtl/wave_generator.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/wave_generator.v, assets/board_projects/boards/wave_generator_board.v, and assets/board_projects/sim/tb_wave_generator.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Run the testbench, select each mode, and explain how phase_step changes frequency. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 275 - 26.2 - 8-point FFT spectrum viewer

Theme and objective	Transform eight signed samples into real and imaginary frequency bins using a radix-2 butterfly pipeline. This is an original Rintronic teaching design. Read rtl/fft8.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/fft8.v, assets/board_projects/boards/fft8_board.v, and assets/board_projects/sim/tb_fft8.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Compare the simulated bins with a hand-calculated impulse and sine wave. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 276 - 26.3 - Streaming FIR noise filter

Theme and objective	Apply an eight-tap moving-average FIR to a signed sample stream while preserving valid/ready timing. This is an original Rintronic teaching design. Read rtl/fir8.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/fir8.v, assets/board_projects/boards/fir8_board.v, and assets/board_projects/sim/tb_fir8.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Inject an impulse and a noisy step; record settling time and explain each tap. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)

BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 277 - 26.4 - Synthetic ECG peak and interval analyzer

Theme and objective	Detect peaks and estimate intervals in a generated ECG-like waveform for educational signal-processing practice; it is not a medical device or diagnostic. This is an original Rintronic teaching design. Read rtl/ecg_features.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/ecg_features.v, assets/board_projects/boards/ecg_features_board.v, and assets/board_projects/sim/tb_ecg_features.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Use synthetic samples only, verify refractory behavior, and state why clinical claims are out of scope. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 278 - 26.5 - Glitch-free PWM LED dimmer

Theme and objective	Latch an eight-bit duty cycle at a PWM period boundary so a real LED never receives a half-updated pulse. This is an original Rintronic teaching design. Read rtl/pwm_dimmer.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/pwm_dimmer.v, assets/board_projects/boards/pwm_dimmer_board.v, and assets/board_projects/sim/tb_pwm_dimmer.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Change duty while running, inspect the waveform, and verify the 0% and 100% edge cases. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 279 - 26.6 - Fixed-point PI motor-control demo

Theme and objective	Compute a bounded integer proportional-integral correction for a simulated plant, including anti-windup. This is an original Rintronic teaching design. Read rtl/pi_controller.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/pi_controller.v, assets/board_projects/boards/pi_controller_board.v, and assets/board_projects/sim/tb_pi_controller.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Step the reference, plot convergence, and identify the effect of each gain. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 280 - 26.7 - Eight-channel post-trigger logic analyzer

Theme and objective	Capture synchronized digital inputs around a trigger and freeze a 16-sample buffer for inspection. This is an original Rintronic teaching design. Read rtl/logic_capture.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/logic_capture.v, assets/board_projects/boards/logic_capture_board.v, and assets/board_projects/sim/tb_logic_capture.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Trigger twice, prove the trigger sample is included, then re-arm the capture. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 281 - 26.8 - UART telemetry transmitter

Theme and objective	Transmit a byte as an 8N1 serial frame with a parameterized baud clock divider. This is an original Rintronic teaching design. Read rtl/uart_tx.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/uart_tx.v, assets/board_projects/boards/uart_tx_board.v, and assets/board_projects/sim/tb_uart_tx.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Decode the simulated line, count every bit, and reject a start request while busy. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)

BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 282 - 26.9 - Industrial sensor alarm with hysteresis

Theme and objective	Qualify a threshold crossing with hysteresis and an invalid-configuration alarm to prevent chatter. This is an original Rintronic teaching design. Read rtl/hysteresis_alarm.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/hysteresis_alarm.v, assets/board_projects/boards/hysteresis_alarm_board.v, and assets/board_projects/sim/tb_hysteresis_alarm.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Sweep the sensor above and below both thresholds and explain why the output does not chatter. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Lesson 283 - 26.10 - CRC-protected packet checker

Theme and objective	Calculate CRC-16/CCITT-FALSE over an enabled byte stream so packet corruption is detectable. This is an original Rintronic teaching design. Read rtl/crc16_stream.v, the matching board wrapper, and its self-checking testbench to understand what is done and how it was implemented.
Complete example	`Simulation files: assets/board_projects/rtl/crc16_stream.v, assets/board_projects/boards/crc16_stream_board.v, and assets/board_projects/sim/tb_crc16_stream.sv. The README documents waveforms, controls, expected results, MPFS-DISCO-KIT pin constraints, and the Libero programming flow.`
Learner action	Verify the 123456789 check vector, pause the stream, and inject one changed byte. Then run the self-checking Icarus Verilog test, review the expected waveform, and record one observation in your lab notebook.
Expected knowledge	The testbench passes and the learner can explain the RTL, waveform, and board mapping
Teaching aid	Original project walkthrough with source preview, signal trace, testbench, and board checklist.
Lab target	Icarus Verilog simulation followed by Microchip PolarFire SoC Discovery Kit implementation
Controls / actions	Run simulation, inspect signals, then map switches and LEDs through the supplied wrapper.
Required lab evidence	Passing self-checking testbench, annotated waveform, timing report, and board observation.

Signals: CLK, RESET, DATA, RESULT, VALID	Interactive inputs: Run testbench, Inspect waveform, Record result, RST
In-app controls: clocked, resettable, multi-bit data	10 guided activities; 10 checks per attempt drawn from 50 generated question variants

PHYSICAL BOARD PATH	Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT, MPFS095T-1FCSG325E)
BOARD EVIDENCE	Use the supplied discovery_io.pdc and discovery_timing.sdc; verify the exact board revision before programming.

Implementation and reference notes

The in-app live graphs are instructional simulations. Physical deployment follows: simulate -> synthesize -> constrain -> timing -> program -> measure. Exported constraint files deliberately retain pin placeholders until the official guide and schematic for the exact board revision have been checked.

Primary student platform: Microchip PolarFire SoC Discovery Kit (MPFS-DISCO-KIT). Advanced transceiver and memory activities may use the PolarFire FPGA Evaluation Kit or PolarFire FPGA Splash Kit when the named peripheral is not available on the Discovery Kit.

Official reference links

Microchip PolarFire SoC Discovery Kit: https://www.microchip.com/en-us/development-tool/MPFS-DISCO-KIT

Microchip PolarFire FPGA Evaluation Kit: https://www.microchip.com/en-us/development-tool/MPF300-EVAL-KIT

Microchip PolarFire FPGA Splash Kit: https://www.microchip.com/en-us/development-tool/mpf300-splash-kit

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